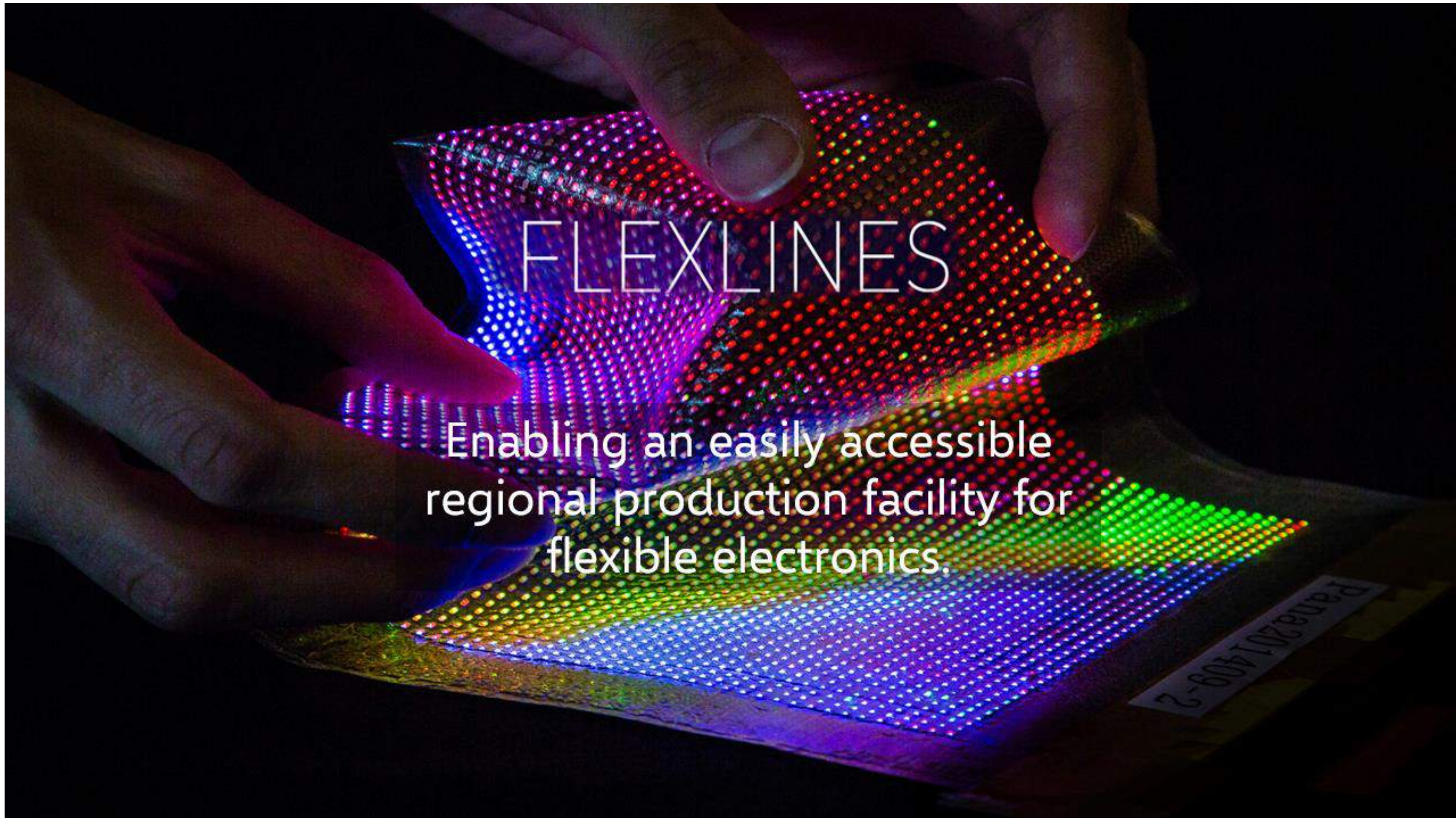
FLEXLINES
FLEXIBLE ELECTRONICS PROTOTYPING

Interreg
Europese Unie
Vlaanderen-Nederland
Europees Fonds voor Regionale Ontwikkeling

FLEXLINES CLOSING EVENT



Agentschap Innoveren & Ondernemen — Vlaanderen is ondernemen — Provincie Oost-Vlaanderen, Voor ieder van ons — Provincie Noord-Brabant — provincie limburg, gesubsidieerd door de Provincie Limburg — Smart Hub Vlaams-Brabant

PROGRAM

- INTRODUCTION
Dieter Therssen, CEO, DSP Valley

- A WORD FROM THE DIRECTOR OF INTERREG
Bram De Kort, Director Interreg Vlaanderen-Nederland

- A WORD FROM THE DEPUTY OF PROVINCE FLEMISH BRABANT
Marlies Vanthyune for Ann Schevenels, Deputy Province of Flemish Brabant

- FLEXLINES ONE-STOP-SHOP:
Romano Hoofman, Program Director, imec

PROGRAM

- LARGE-AREA SHEET-2-SHEET THIN FILM TRANSISTOR PILOT LINE INFRASTRUCTURE
Auke Jisk Kronemeijer, Senior Researcher & GEN1 TFT Pilot Line Manager, TNO/Holst Centre

- UNDERSTANDING AND IMPROVING TFT PERFORMANCE:
Rene Janssen, Professor Molecular Materials and Nanosystems, TU/E

-- 5 min BREAK --

- CIRCUIT DESIGN TECHNIQUES WITH InGaZnO THIN-FILM TRANSISTORS FOR LARGE AREA ELECTRONICS:
Mohit Dandekar, research assistant, KU Leuven

PROGRAM

- PRINTED ELECTRONICS FOR THERMOFORMING AND INJECTION MOULDING:

Margreet De Kok, Program manager structural electronics, TNO/Holst Centre

- THE EFFECT OF OVERMOULDING ON RELIABILITY OF FLEXIBLE ELECTRONIC CIRCUITS:

Mona Bakr, Researcher, imec CMST

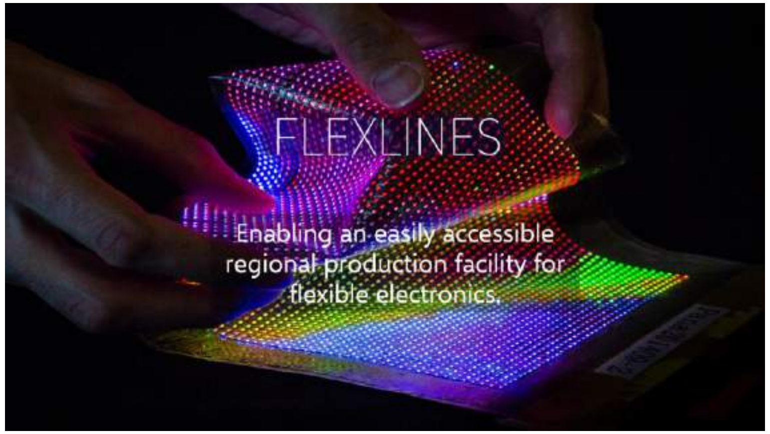
- INJECTION OVER-MOULDING FLEXIBLE ELECTRONICS WITH ENGINEERING THERMOPLASTICS:

Yibo Su, Scientist, Brightlands Materials Center

- CONCLUSIONS / CLOSING REMARKS - ONE-STOP-SHOP REMINDER

Romano Hoofman, Program Director, imec

Dieter Therssen, CEO DSP Valley



A regional collaboration

Objectives

- Expansion of a Flexible Electronics pilot infrastructure. Operationalization of essential production investments and improvement of design and production processes.
- Set-up of a 'one-stop-shop' for the realization of prototypes of Flexible Electronics applications.
- Realisation of a number of demonstrators
  - as the first validation for the deployed design and manufacturing assets
  - as showcases, to inform the ecosystem about the possibilities

A regional collaboration

Holst Centre

Open Innovation by imec and TNO

KU LEUVEN

Cmst

TNO innovation for life

Brightlands Materials Center

imec.IC-link

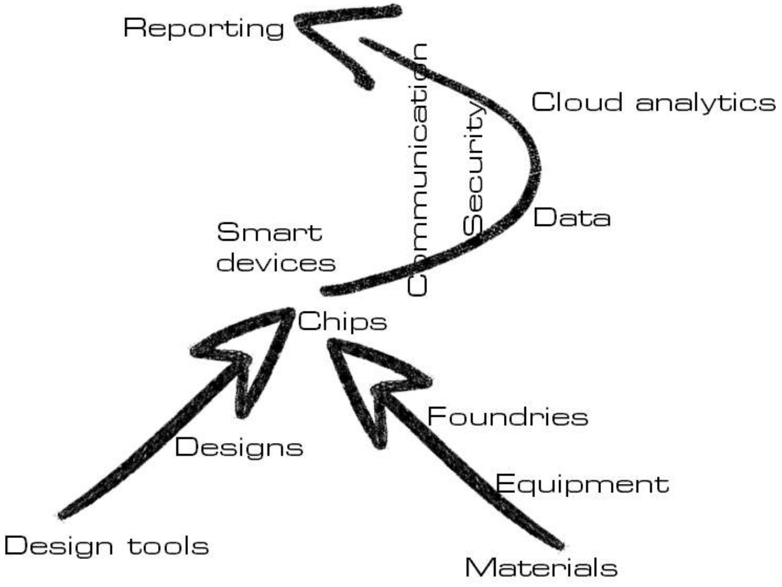
imec

TU/e

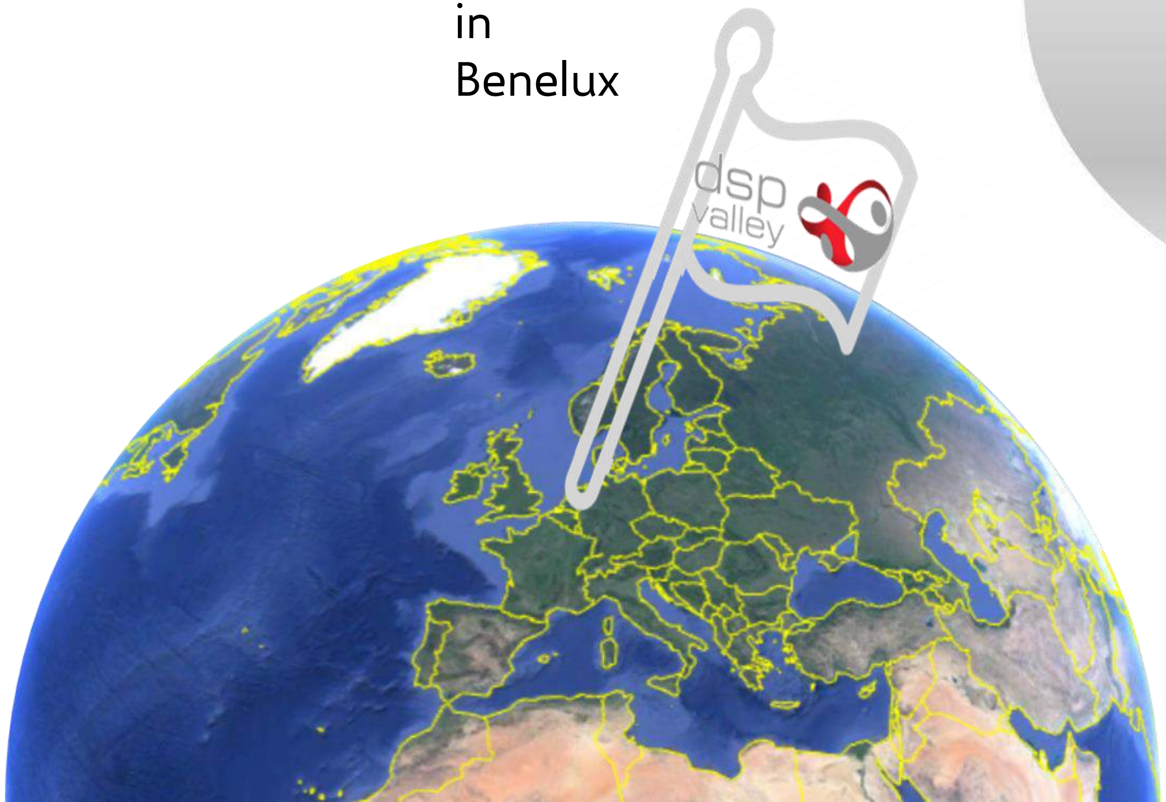
dsp valley

breeding digital business

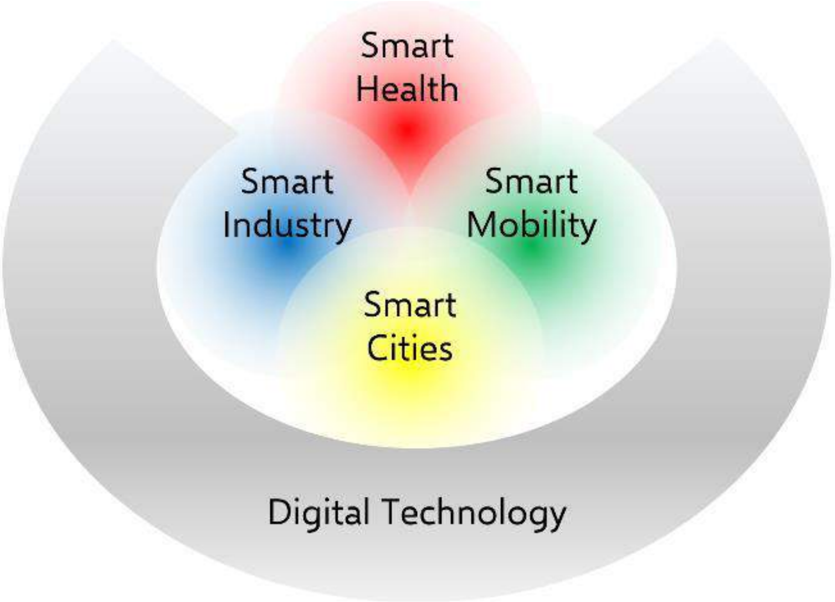
the digital value chain



150
Members
in
Benelux

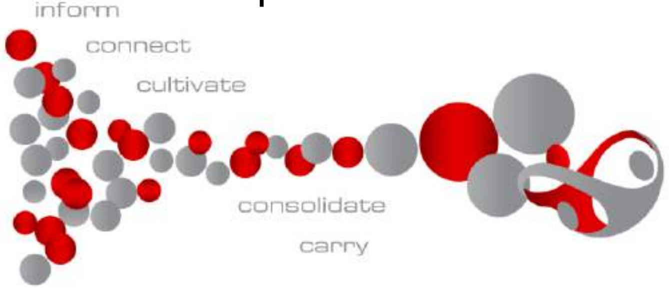


5 programmes



collaborative bizdev

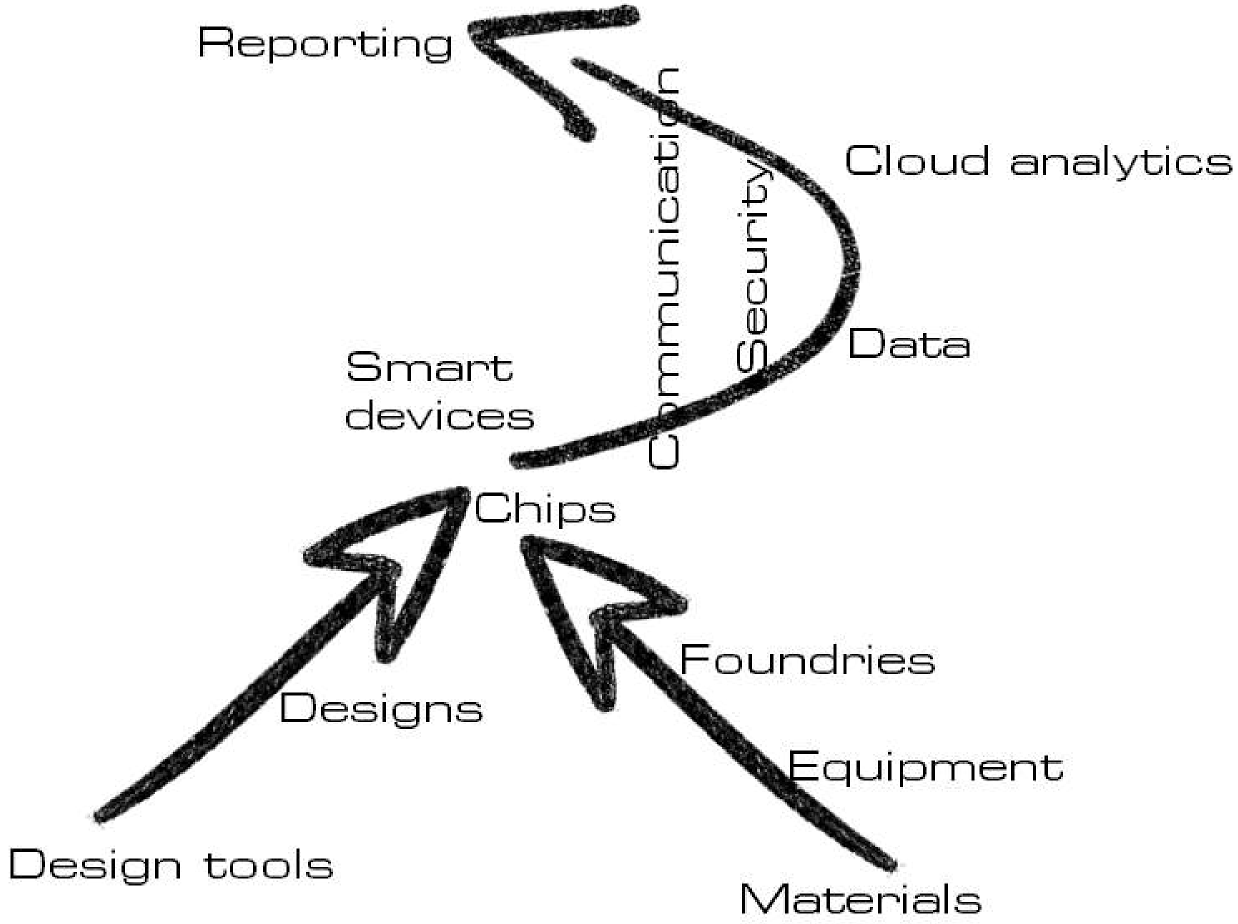
1 process



Flexlines

Scope

- Flexlines addresses the entire physical realization part of novel formable electronics and their embodiment in devices.
- Design tools (modeling, simulation), design, fabrication steps, flexible electronics, integration in over-moulded assemblies.



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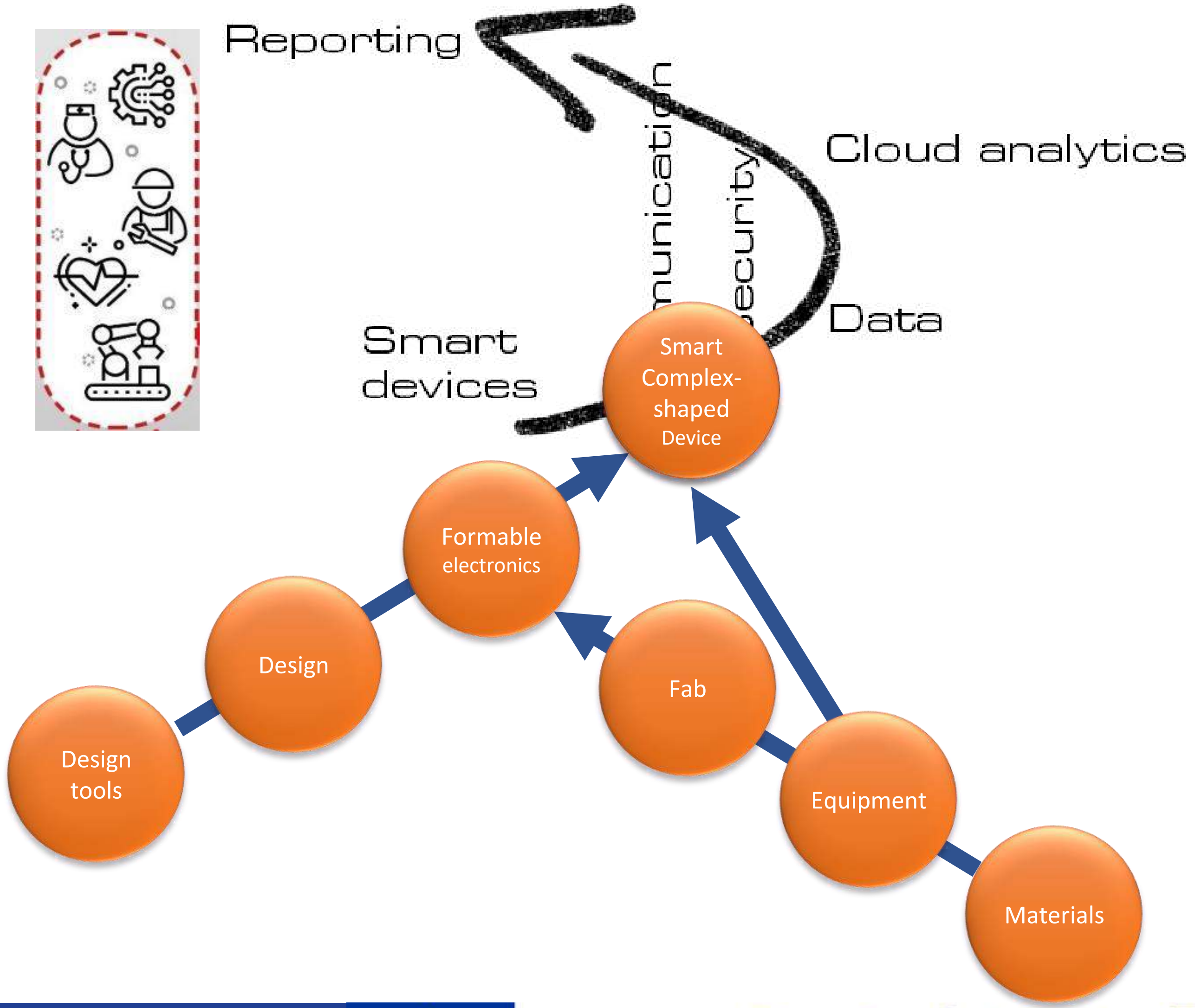


Flexible electronics projects

https://www.smartx-europe.eu/application/

Projects contributing technology:

~1 MIO EUR cascade funding

~1 MIO EUR cascade funding

FLEXLINES
FLEXIBLE ELECTRONICS PROTOTYPING

Prototyping infrastructure and design-tools in Benelux: at your disposal for trials with Interreg subsidy.

SmartEEs
BRINGING FLEXIBLE ELECTRONICS PRODUCTS TO LIFE

A total of ~2 Mio EUR to support projects at your company.

SMARTX
EUROPEAN SMART TEXTILES ACCELERATOR

Integration in textiles.

PORTUGUESE TEXTILE CLUSTER

citeve TEXTILE TECHNOLOGY

CENTEXBEL

institut FRANÇAIS de la MODE

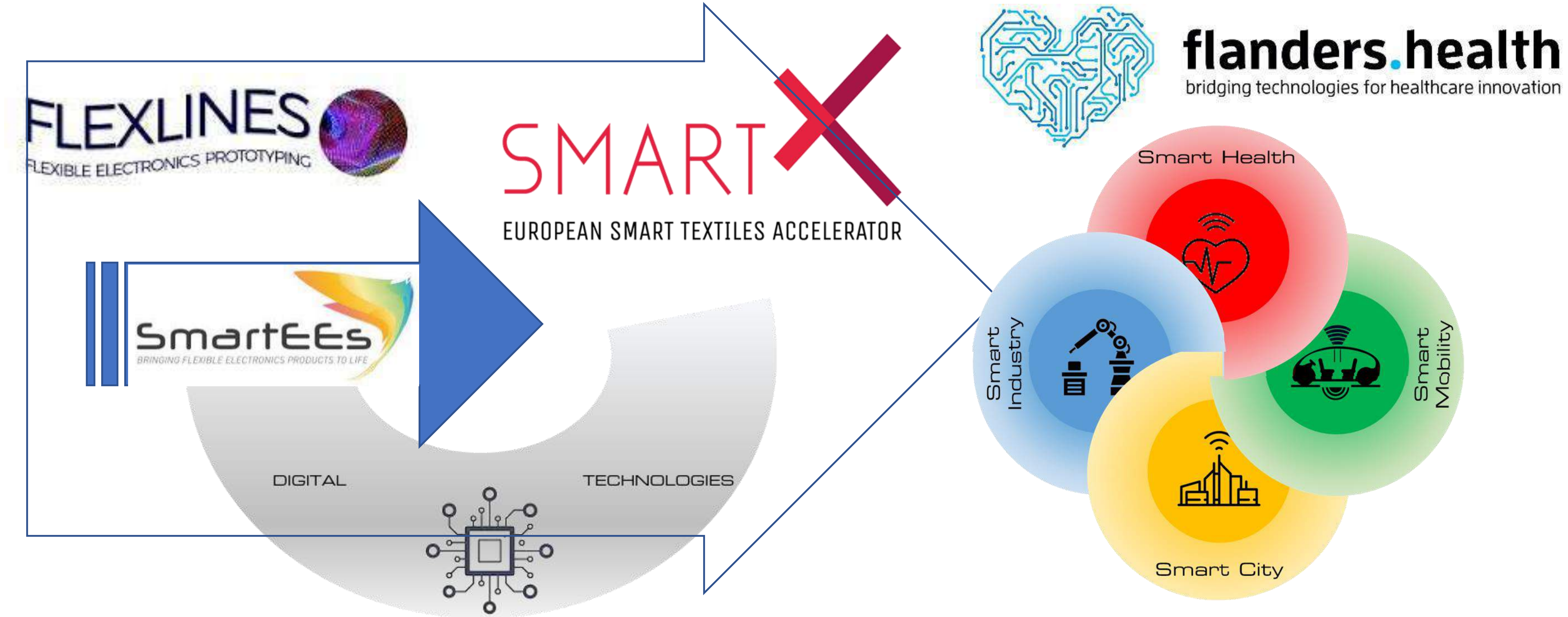
DITF DEUTSCHE INSTITUTE FÜR TEXTIL- UND FASERFORSCHUNG

po.in.tex Polo Innovazione Tessile

https://smartees.eu/open-call-smartees2/

Flexible electronics projects

Into applications that NEED flexible/wearable:



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FLEXIBLE ELECTRONICS PROTOTYPING

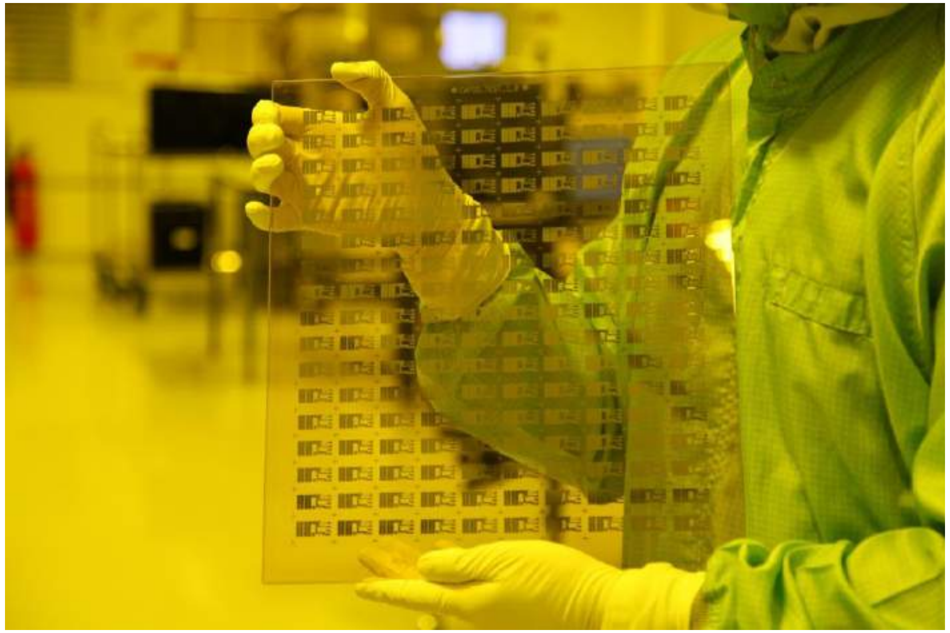
Interreg
EUROPESE UNIE
Vlaanderen-Nederland
Europees Fonds voor Regionale Ontwikkeling

Thank you!

AGENTSCHAP INNOVEREN & ONDERNEMEN
Vlaanderen is ondernemen
Provincie Oost-Vlaanderen Voor ieder van ons
Provincie Noord-Brabant
provincie limburg gesubsidieerd door de Provincie Limburg
SMART HUB VLAAMS-BRABANT

FLEXLINES One-Stop-Shop

Romano Hoofman, imec



Easy access to the fabrication of flexible electronics prototypes

Main objective

"To create a one-stop service, where academia and companies can realize their ideas in flexible and cheap electronics-applications."

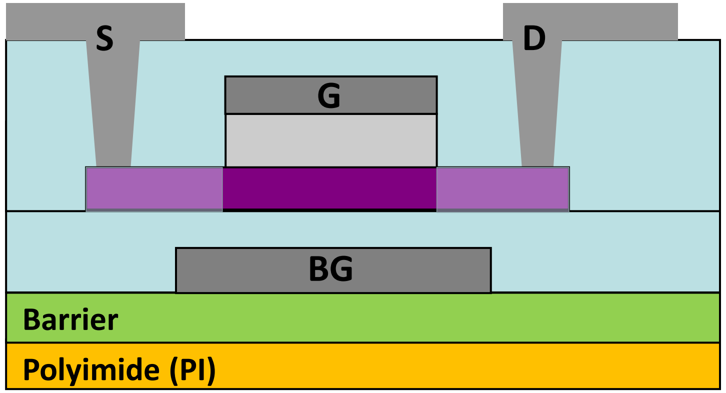
- In order to achieve this, the following is needed:
  - Further maturing of the technology,
  - Development of a compliant design process flow,
  - Reaching out to customers for development of new applications.

What / how / who?

- What will be offered?
- How will it be offered?
- Who is the customer?

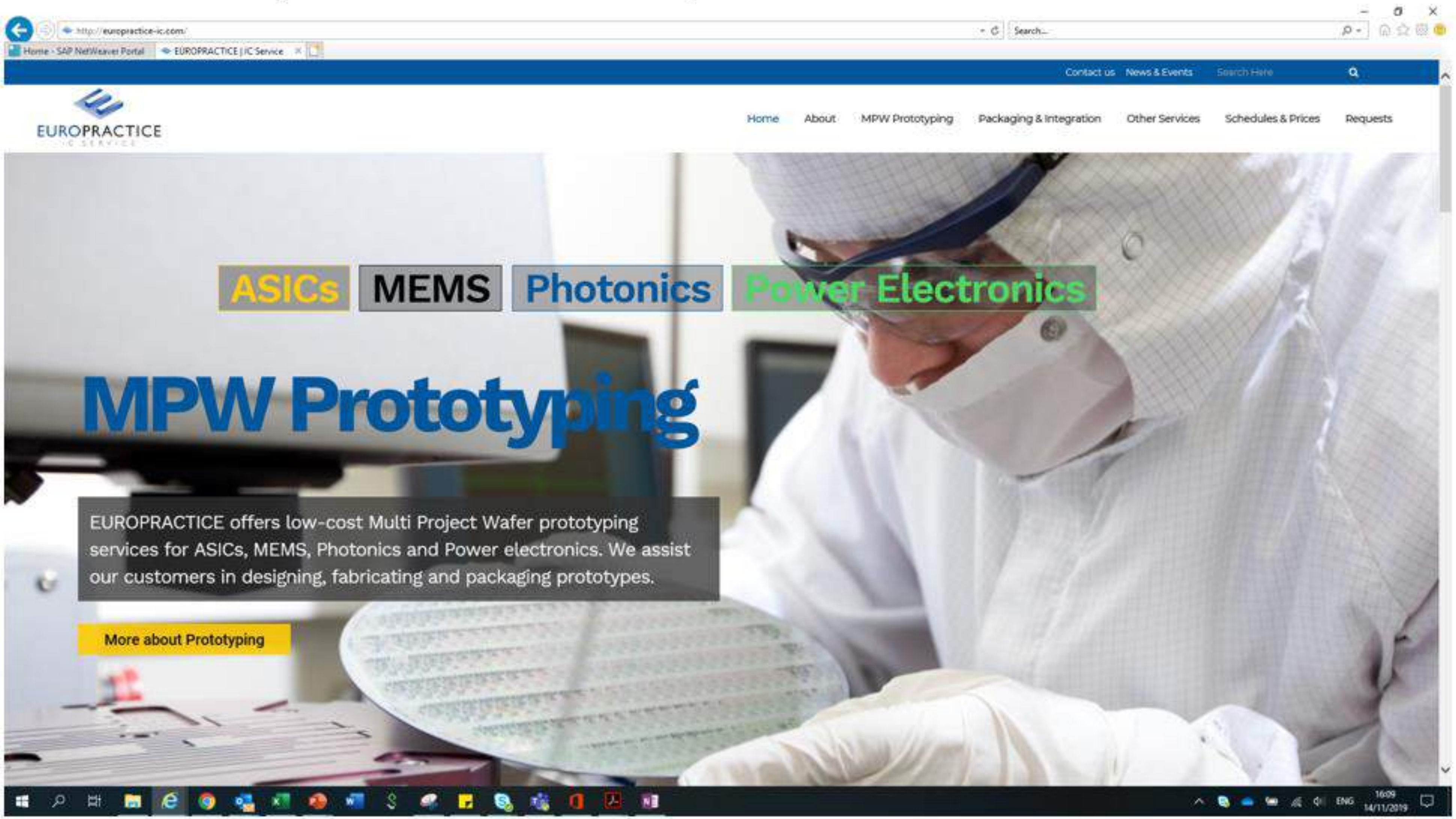
What ?

- TFT process technology



The "Europractice" concept

How ?

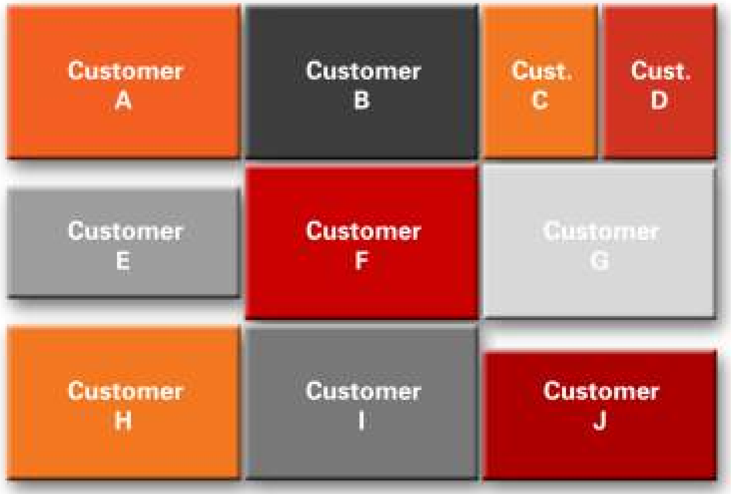


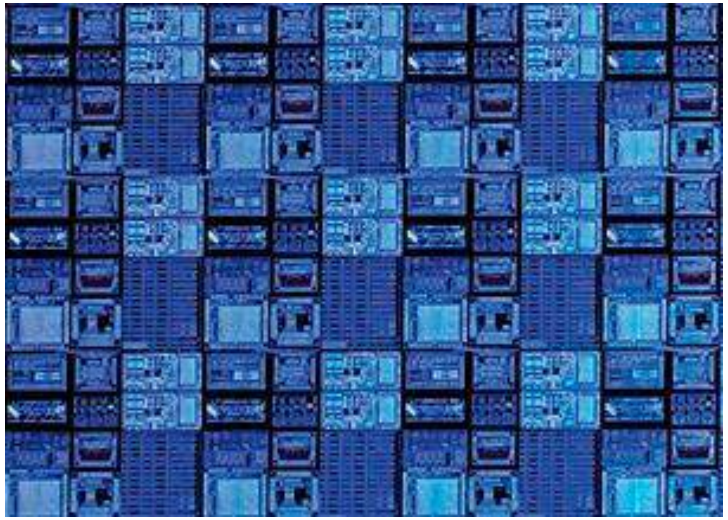
The *“Europractice”* concept

- Launched by EU in 1995 to enhance European competitiveness in global market – collaboration of several European Research institutes – offering of industrial technologies (not easily accessible for prototyping)
- Facilitate access to Si technologies (ASIC, MEMS and PIC) and packaging
- Multi-project wafer approach to lower prototyping cost
- Access to design tool software (packages) for academics

MPW service for flexible electronics

- Multi-customer project services could also be made available for flexible electronics (*if needed*), such that the fabrication cost can be lowered by sharing multiple customer prototypes on the same production run.





Who ?

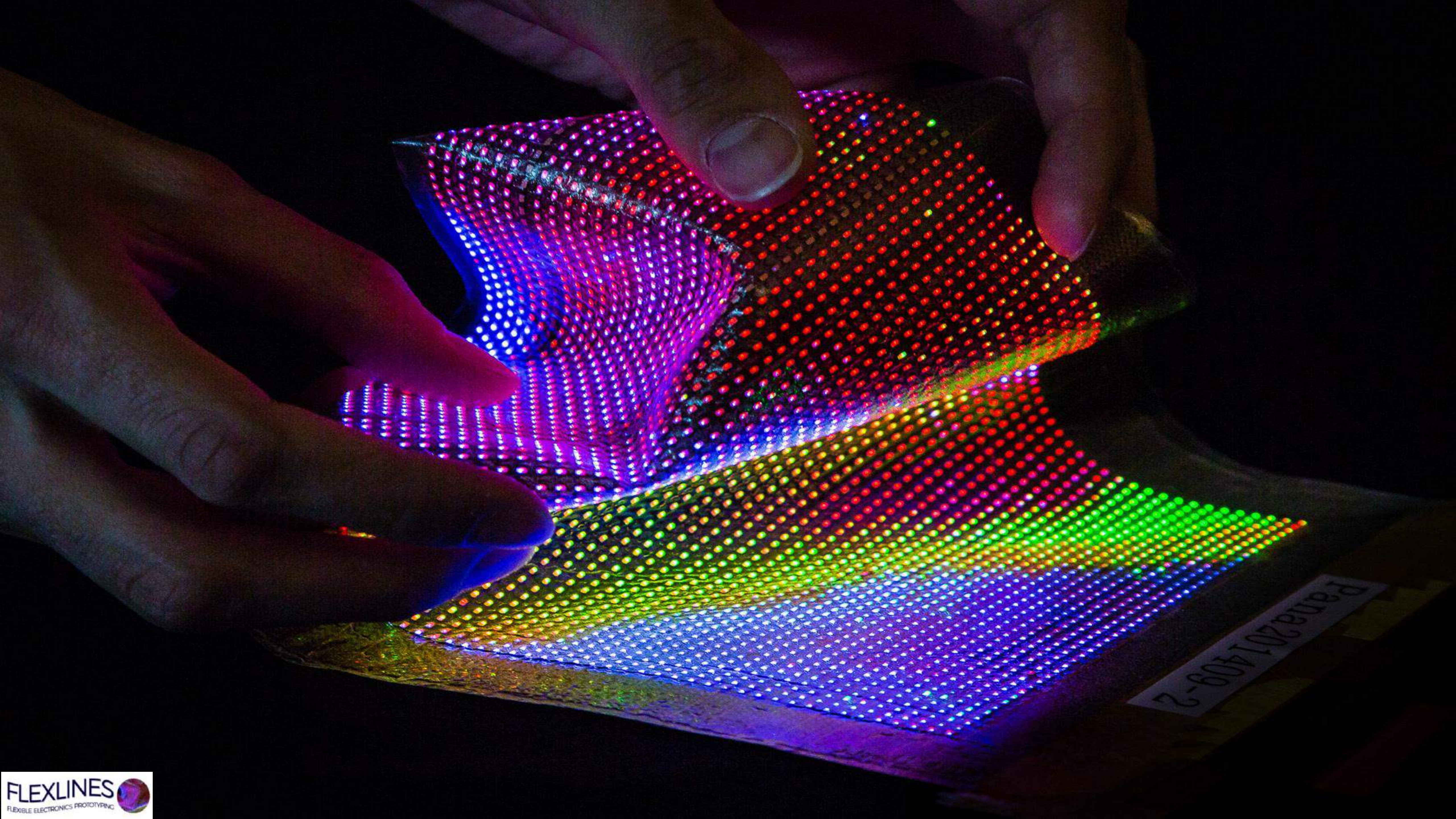
- In the pilot phase:
  - Experienced designers from academic institutions

- After the project:
  - Companies who are (un)familiar with underlying technologies, and their business idea can be realized using these technologies.
    - Additional design support will be offered (at cost)

Leverage

- FLEXLINES utilizes the already existing ecosystem of the project partners.

  - FLEXLINES benefits from the many years experience of imec IC-link and EUROPRACTICE (the one-stop-shop for traditional ICs, MEMS and Si-Photonics)



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Large-Area Sheet-2-Sheet Thin Film Transistor Pilot Line Infrastructure

Auke Jisk Kronemeijer
Program Manager, TNO / Holst Centre

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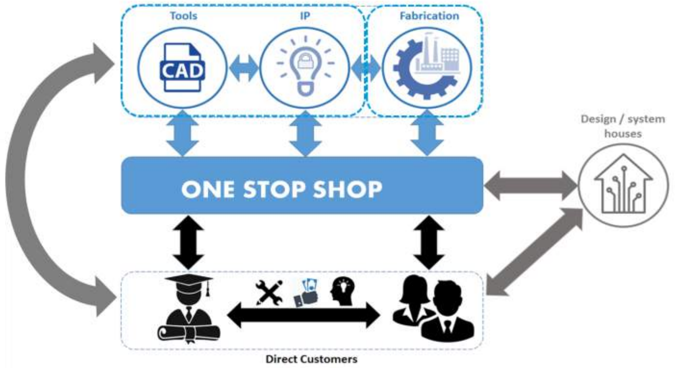
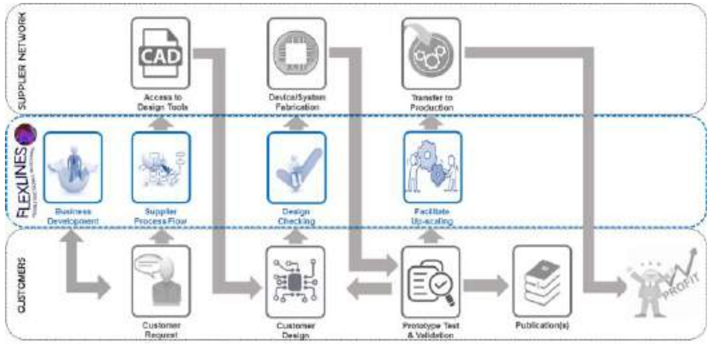
- One-Stop-Shop

  Partnership Cooperation Model





- Core Offer

  Design & Realization Multi-project
  FPD Sheets Electronics-on-Foil

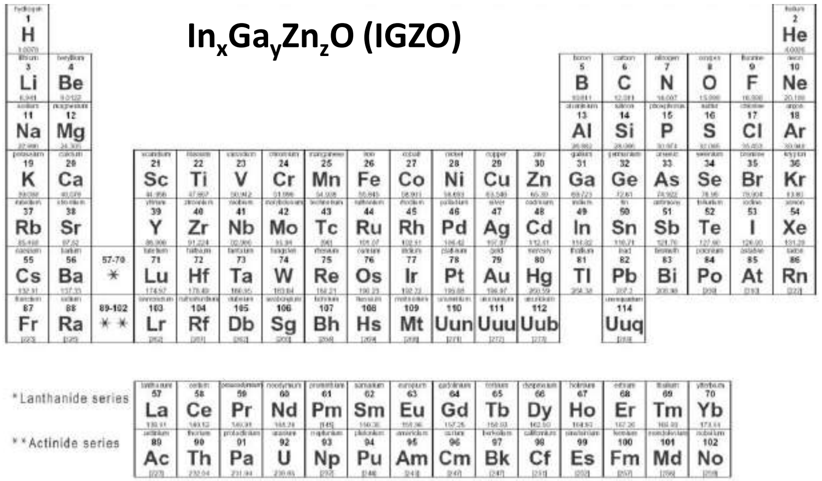
- Optional Offer
  - Integration Technologies

Oxide Transistor Arrays on Plastic

A Key Enabler of Flexible Electronics

Holst Centre R&D TFT Technology

- a-IGZO Oxide Thin Film Transistors



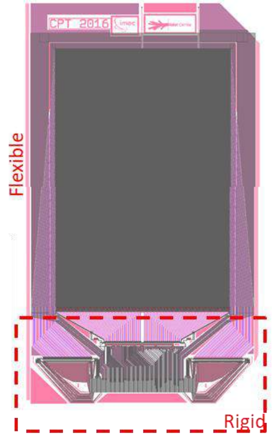
Information Display **36** (3), 9-13 (2020)

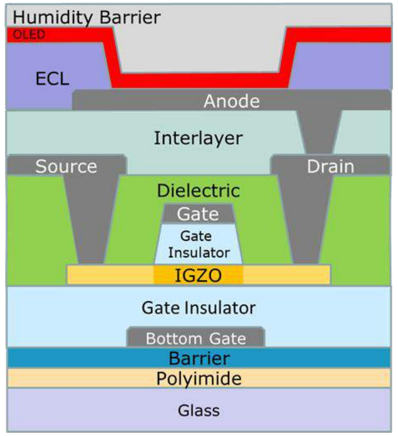
MANUFACTURING FACILITY	FAB SIZE
BOE (B17)—Wuhan, China (a-Si:H TFT/oxide + WOLED*)	Gen 10.5
China Star (T7)—Shenzhen, China (a-Si:H TFT/oxide + WOLED)	Gen 10.5
Mantix Display Technology—Putian, China (a-Si:H/oxide TFT)	Gen 6
Foxconn/SDP—Kameyama, Japan (oxide TFT)	Gen 6
Foxconn/SDP—Kameyama, Japan (oxide TFT)	Gen 8
LG Display (E2)—Paju, South Korea (LTPO)	Gen 4.5
LG Display (P8)—Paju, South Korea (oxide TFT)	Gen 8.5
LG Display (P9)—Paju, South Korea (oxide TFT)	Gen 8.5
LG Display—Guangzhou, China (oxide TFT)	Gen 8.5
LG Display (P10)—Paju, South Korea (oxide TFT)	Gen 10.5
Panda—Nanjing, China (oxide TFT)	Gen 8.5
Panda—Chengdu, China (oxide TFT)	Gen 8.6+
Royole—Shenzhen, China (oxide + OLED)	Gen 5.5
Samsung (A2)—Asan, South Korea (LTPO)	Gen 5.5
Foundry or development facility	
dpiX—Colorado Springs, Colorado	
Flexible Electronics & Display Center—Tempe, Arizona	
Holst Centre—Eindhoven, Netherlands	
Semiconductor Energy Laboratory—Kanagawa, Japan	

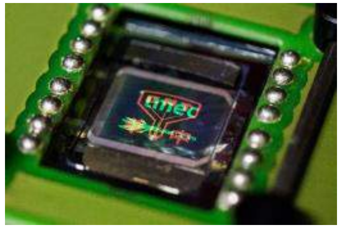
Amorphous n-type Oxide Semiconductor with Increased Install-Base and Existing Products on Display Market

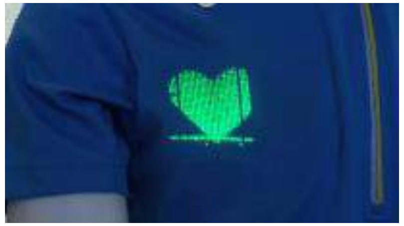
Application Prototyping Platform

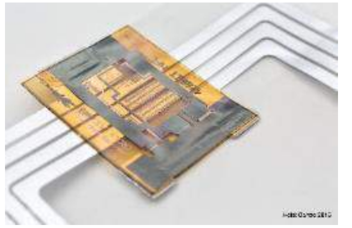
- Flexible Displays
- Flexible Imagers
- Flexible Circuitry
- ….

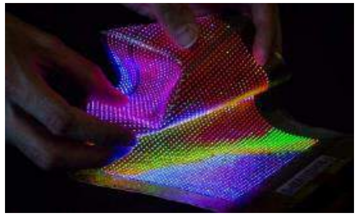


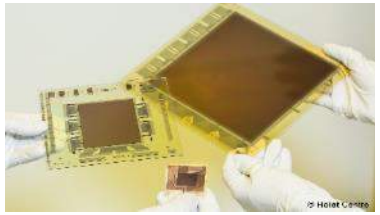






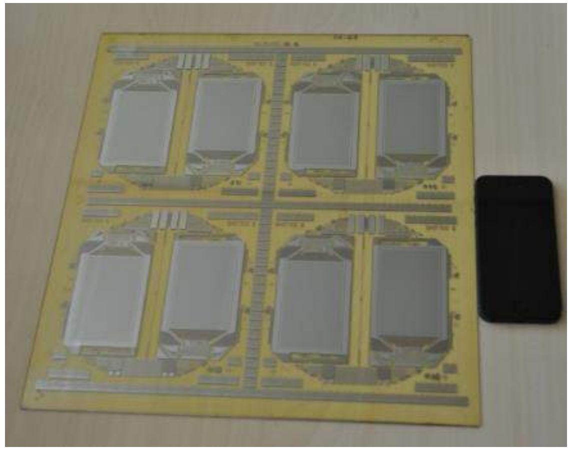


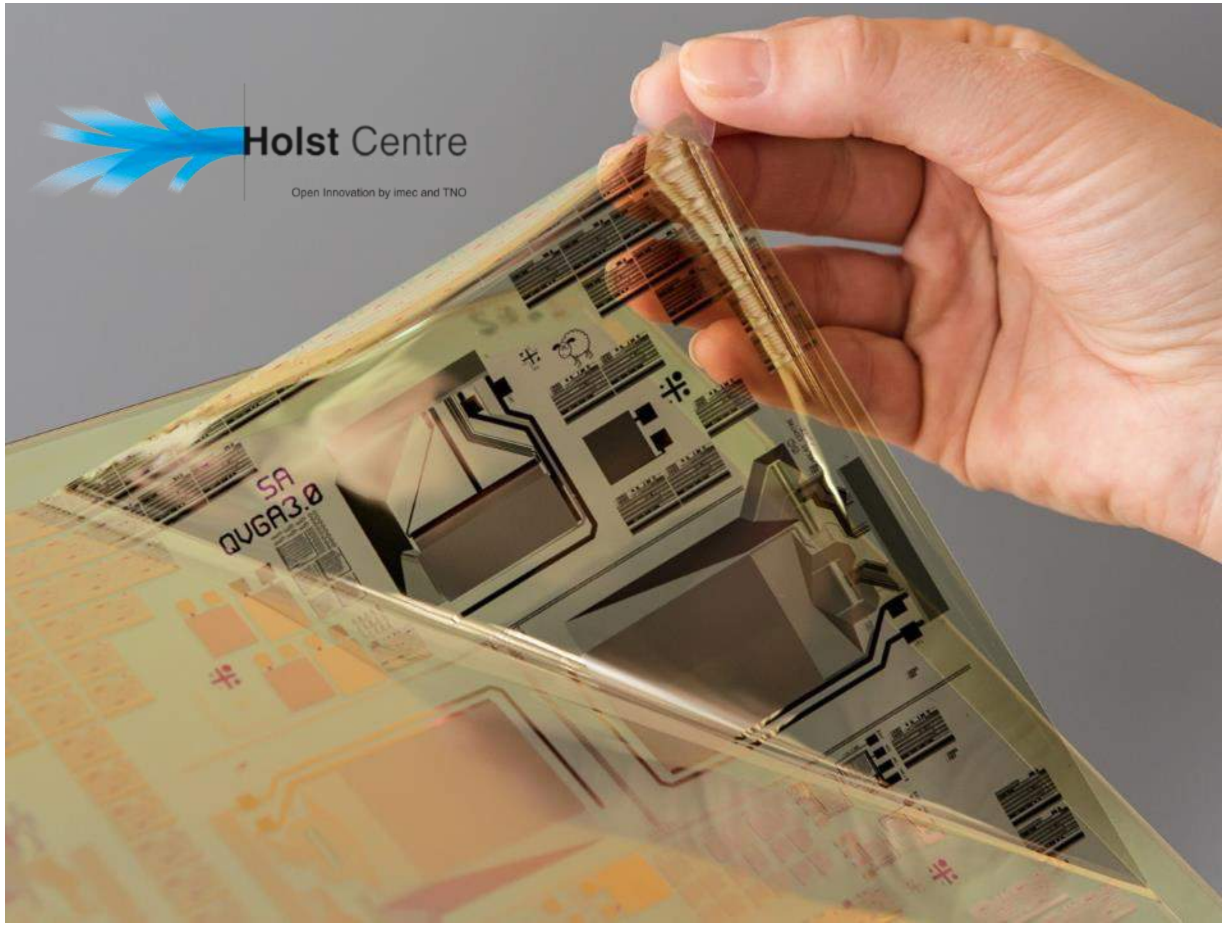




R&D Pilot Line: Size & Applications

- 320x352 mm Glass Substrates
- Temporary Bonding of Laminated or Spin-on Foils for Flexible Electronics
- a-IGZO Semiconductor
- FPD-compatible Processes
- Mechanical & Laser Debonding
- Prototypes:
  - Displays
  - Imagers
  - Circuits

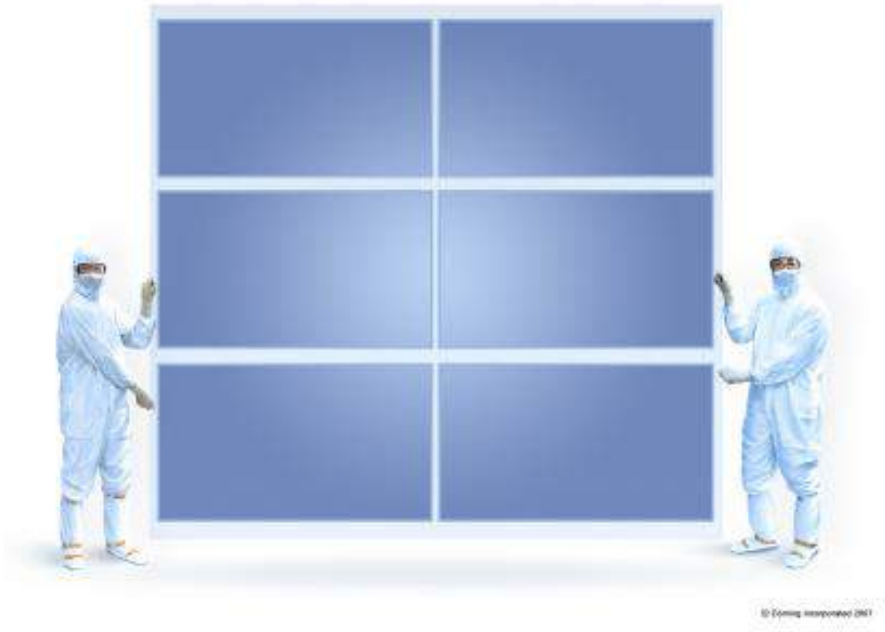


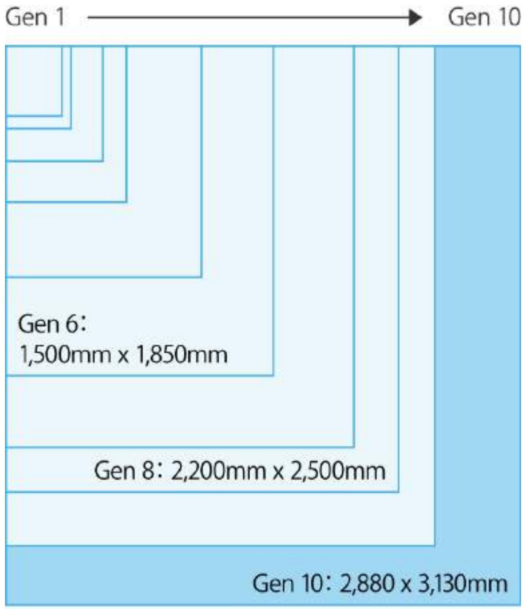


Scalable to Mass Manufacturing

- Flat Panel Display Fabrication Plants

Sharp Gen10 plant, Sakai City

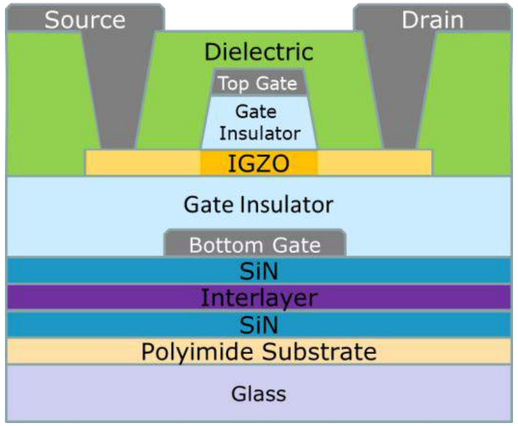


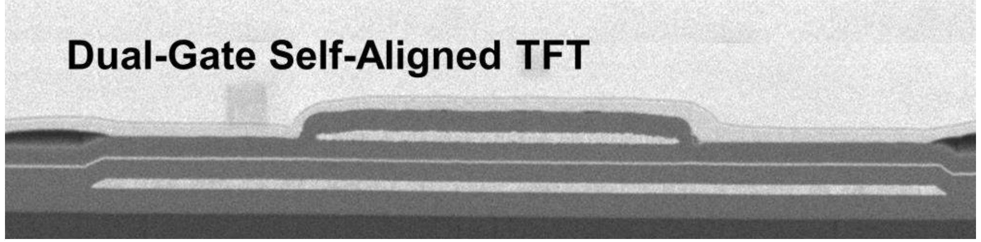


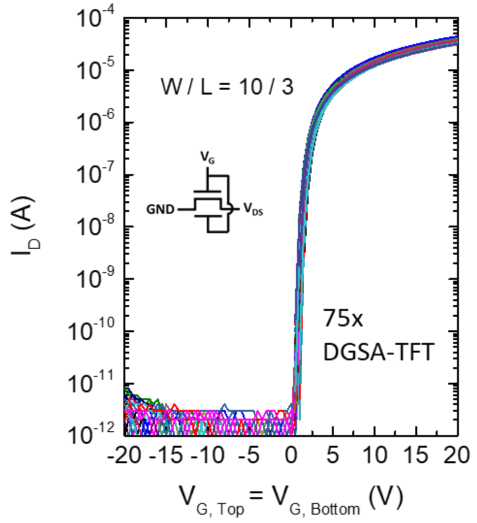
Holst Centre R&D Pilot Line Facilities

Flexlines: New Infrastructure (1)

- Centralisation of TFT Process Flow *in* Eindhoven
  - Move a-IGZO Sputtering from Leuven (BE) to Eindhoven (NL)
- Installation & Release of New 32 x 35 cm Sputter Tool
  - 2 Chambers, 4 Targets
    - a-IGZO
    - ITO
    - MoCr
    - AlTi
- No Transport Leuven / Eindhoven Needed
  - Batch Throughput Time Decreased by 1 Week



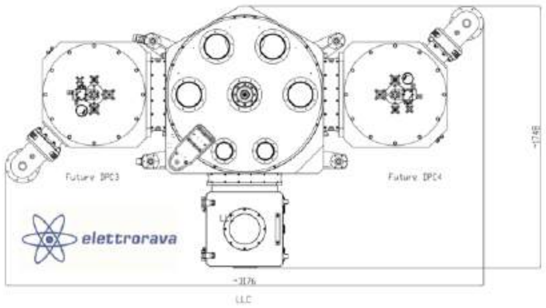


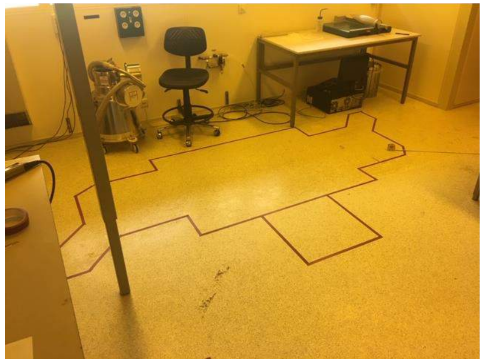


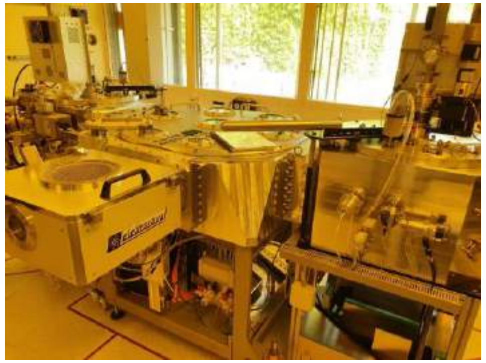
Flexlines: New Infrastructure (2)

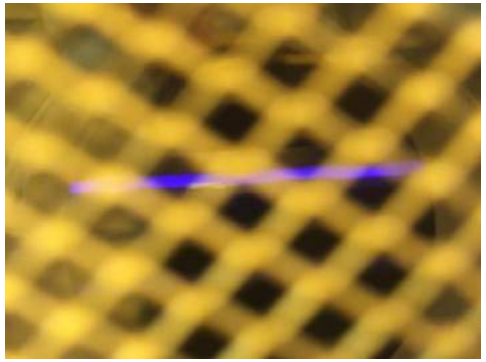
- Centralisation of TFT Process Flow *within* Eindhoven
  - Transfer of PECVD Process from Philips Innovation Services to Holst Centre
- Installation and Release of New 32 x 35 cm PECVD Tool
  - European Tender, Unforeseen Court Case, Assembly at Supplier, Installation at Holst Centre
  - Process Release – Delayed due to Court Case and Corona

(PInS Decommission as Planned, No PECVD Q4 2020 – Impacting Flexlines)



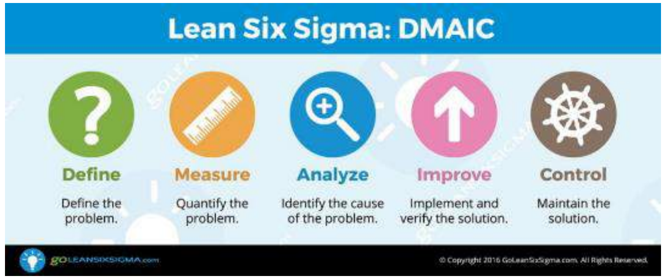






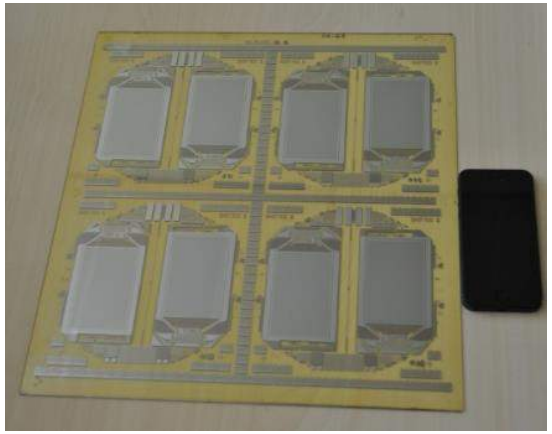
Implementation of Process Monitoring & Technology Improvement

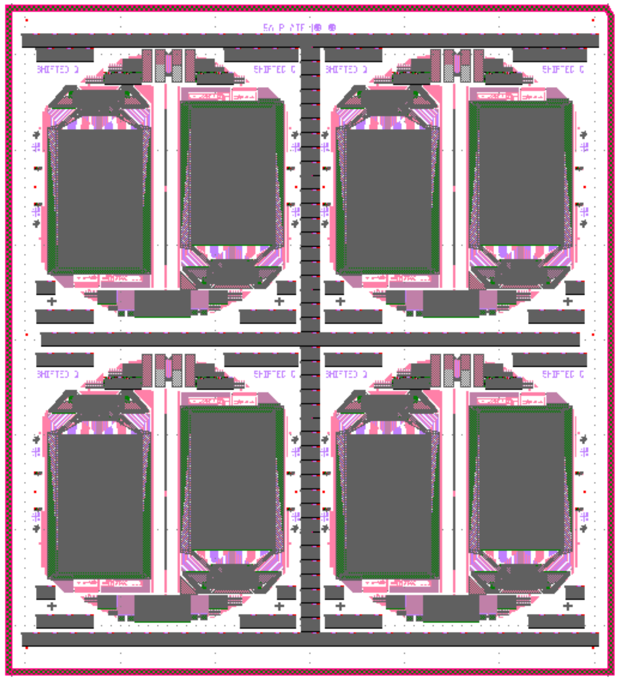
- Implementation of Six Sigma Methodology
  - Black Belt / Green Belt Courses for Pilot Line Employees

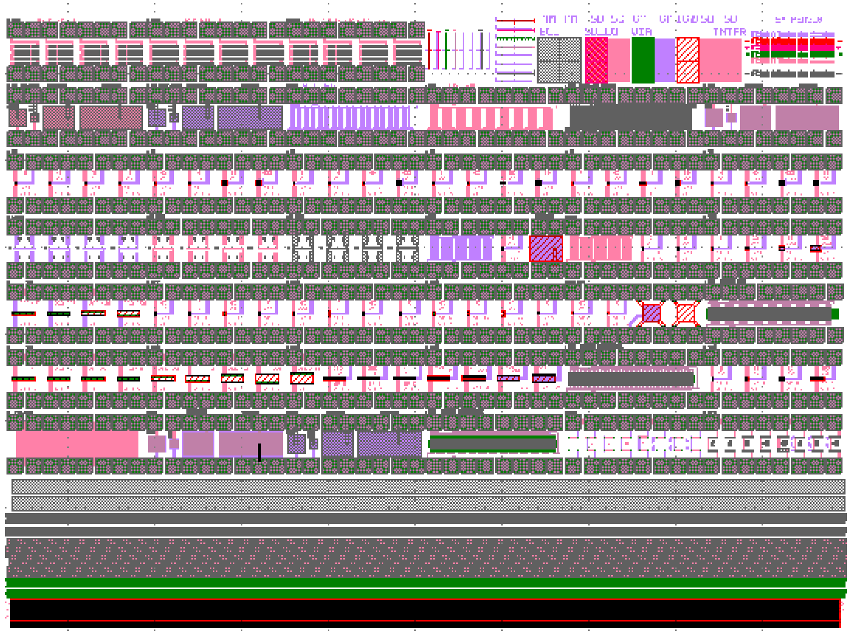


Implementation of Process Monitoring & Technology Improvement

- Implementation of Six Sigma Methodology
  - Creation of Monitoring Dashboard







Implementation of Process Monitoring & Technology Improvement

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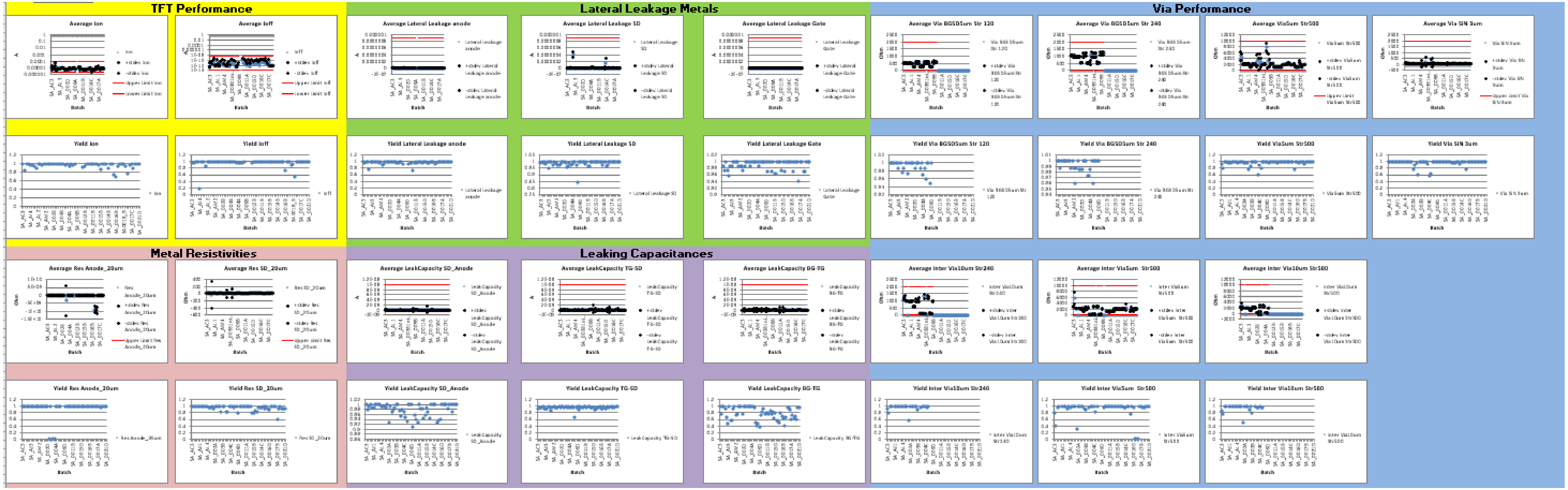
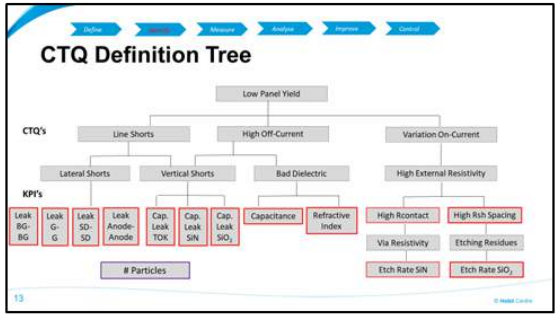
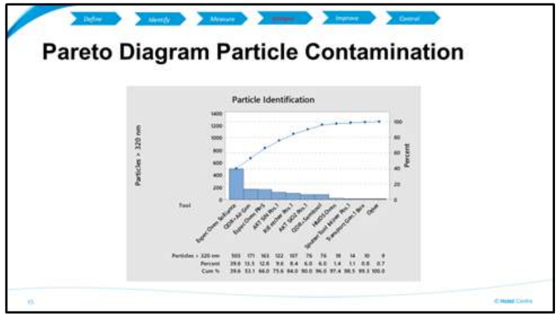
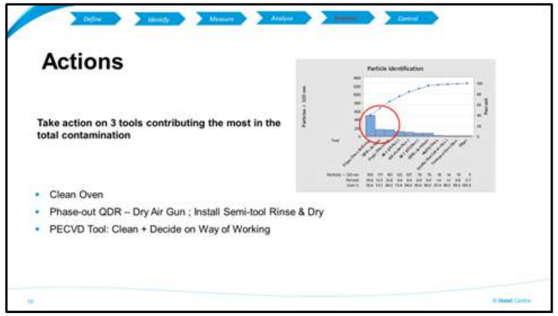


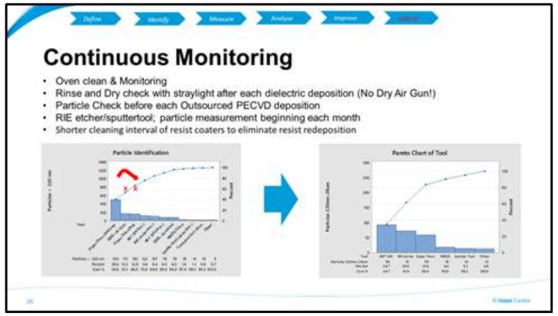
Implementation of Process Monitoring & Technology Improvement

- Implementation of Six Sigma Methodology
  - Improvement Baseline Technology





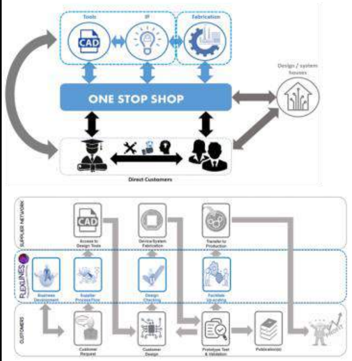




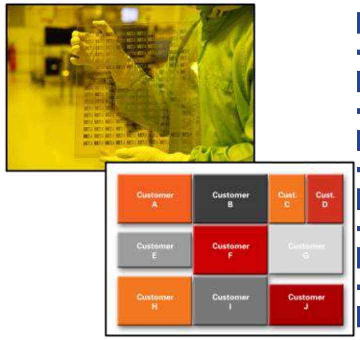
Flexlines Portfolio

- TFT Technology Employed for the Realization of Prototypes

- One-Stop-Shop
  Partnership Cooperation Model



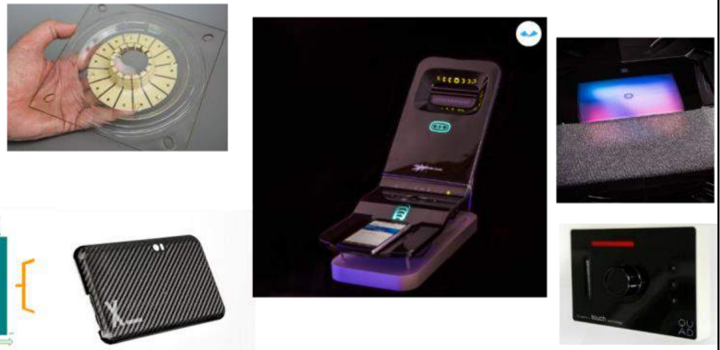
- Core Offer
  Design & Realization Multi-project FPD Sheets Electronics-on-Foil

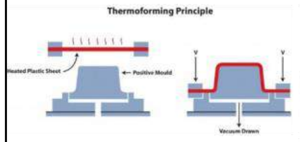


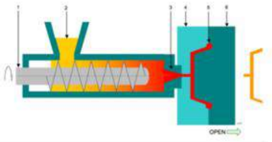
- Optional Offer
  - Integration Technologies

Integration Technologies

- Scale-up to Pilot Fabrication
  - Inlay Lamination
  - Encapsulation
  - Injection Moulding
  - Thermoforming
  - Textile Integration
  - 3D Printing

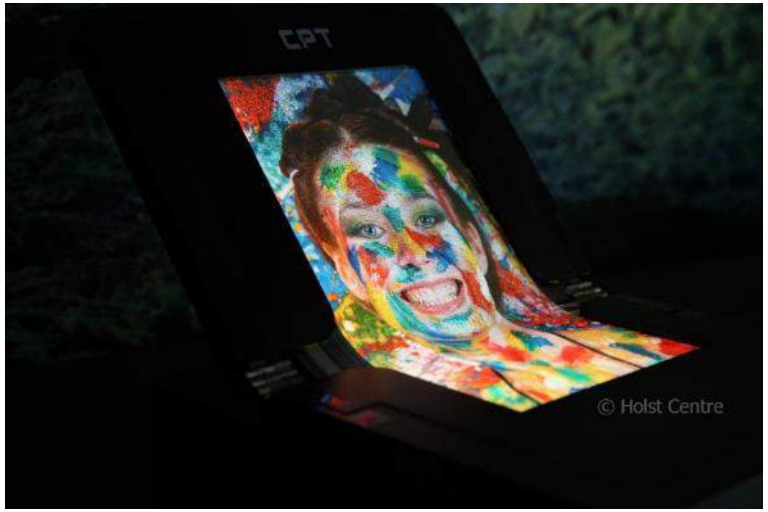


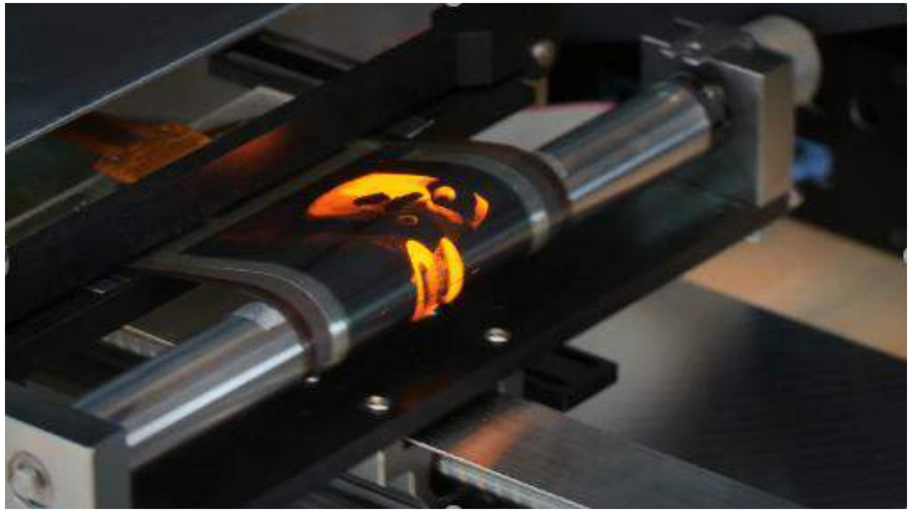




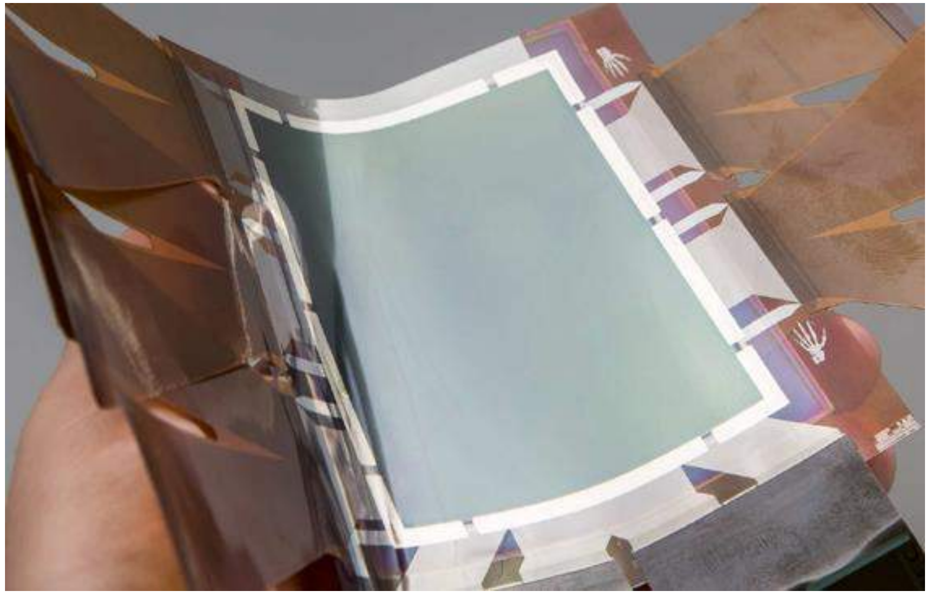
Providing Companies in the Flanders – Netherlands Region with Access to these Technologies for Prototyping

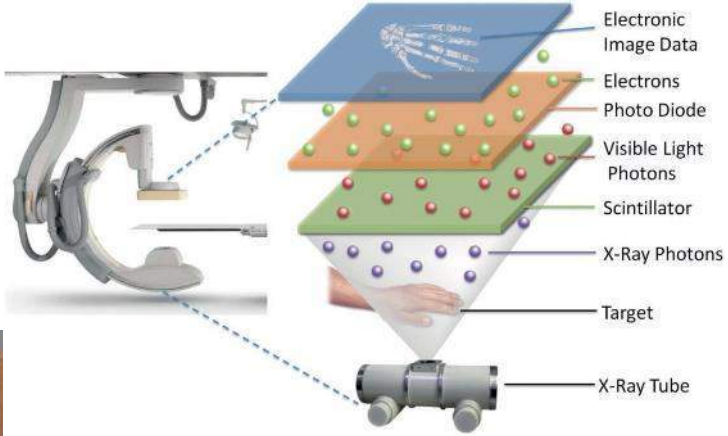
Flexible AMOLED Displays

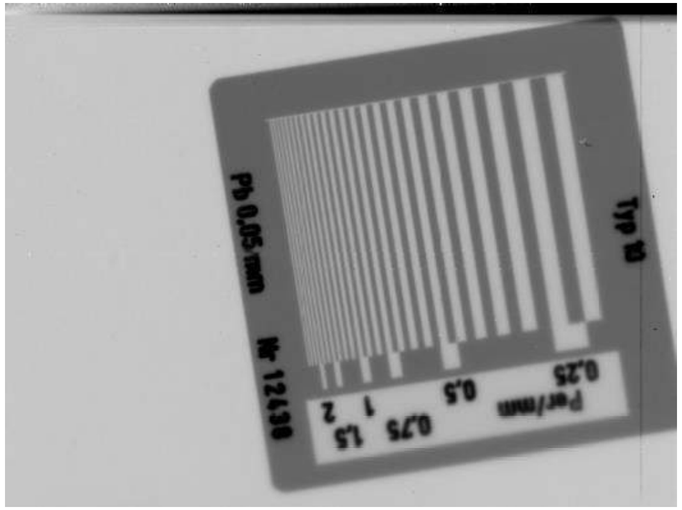




Flexible X-Ray Detectors





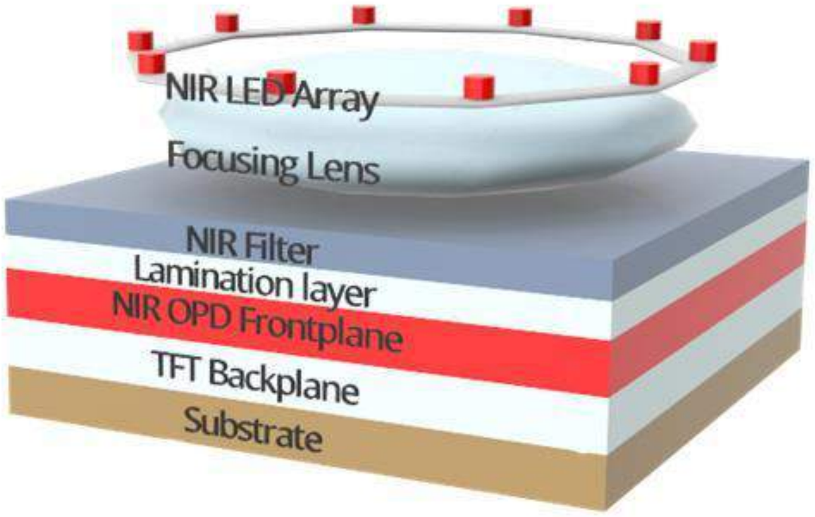


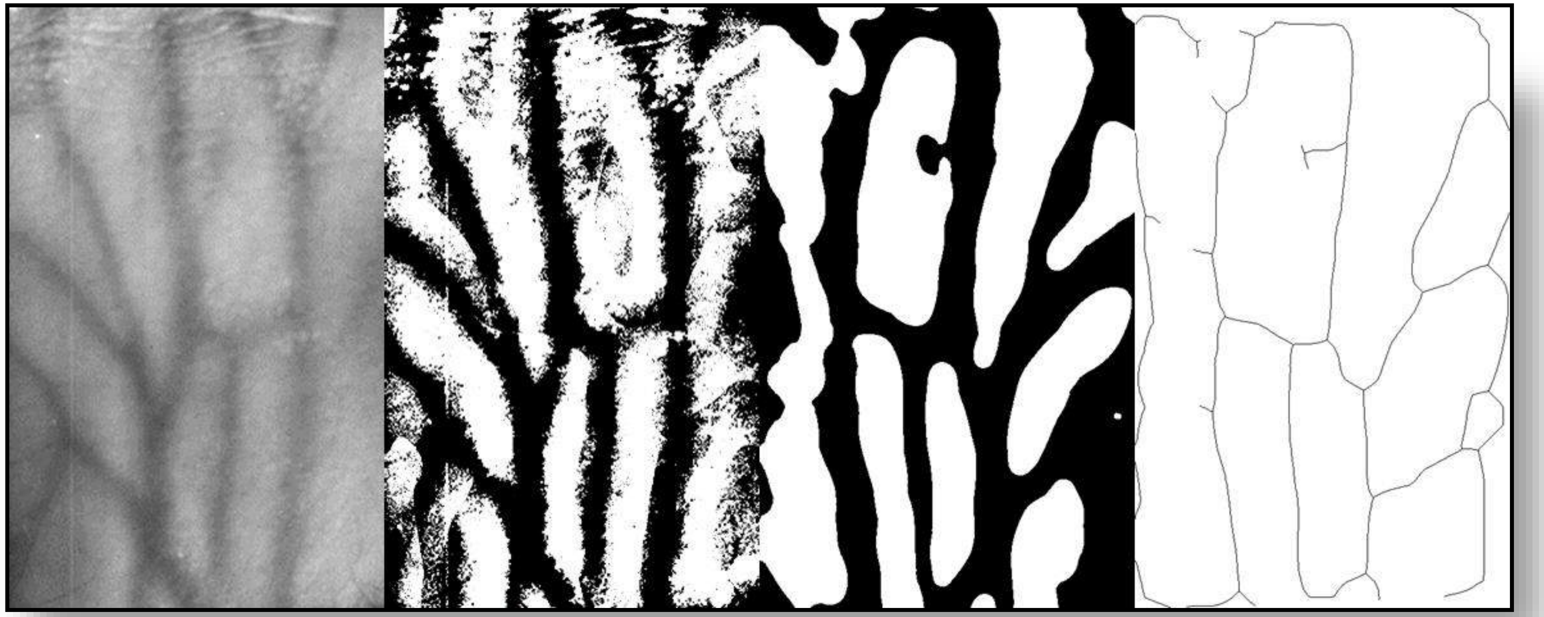
Transparent Fingerprint Scanners

SID
SOCIETY FOR INFORMATION DISPLAY

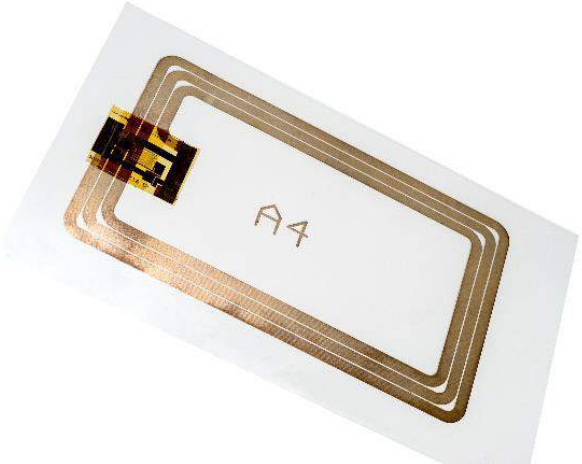
DISPLAY WEEK
SAN JOSE 2019

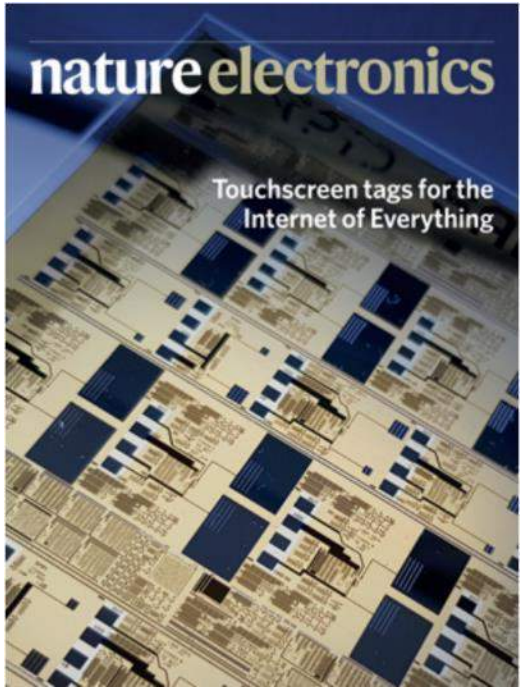
Near-Infrared Vein Detectors



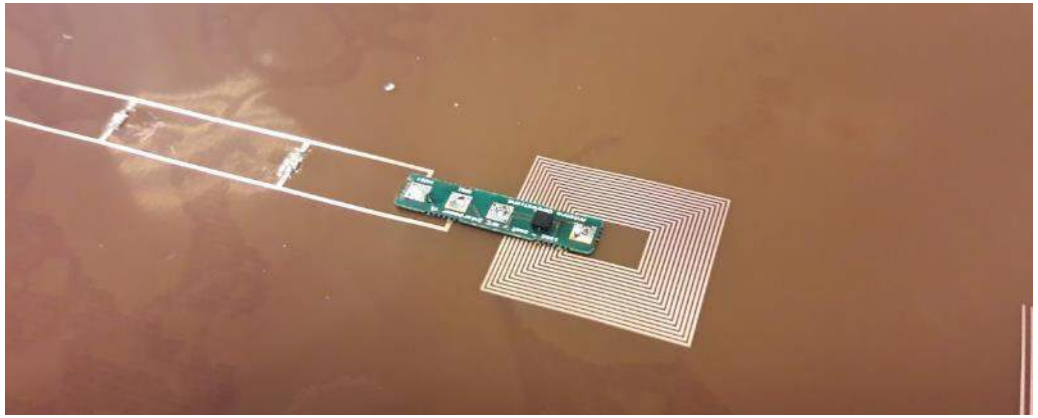


Electronic Tags in Paper

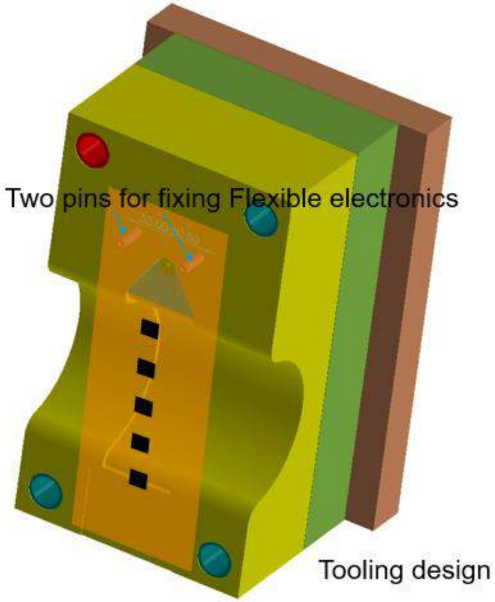




Injection Moulded Circuitry & Components (1)



Injection Moulded Circuitry & Components (2)



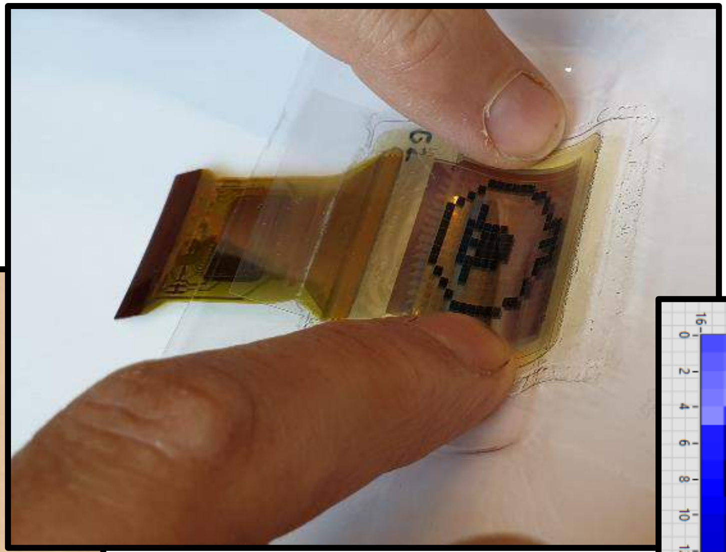
Electronics, Graphics & Component Assembly

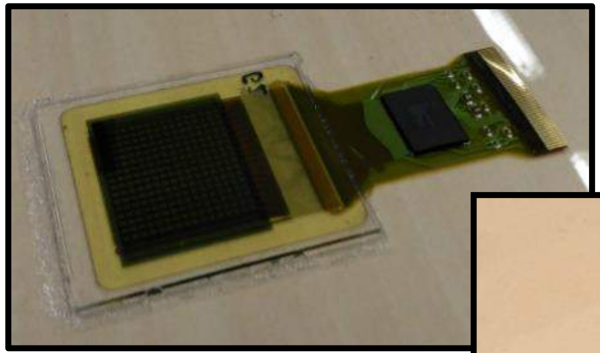
Overmoulding of Flex-Foils

Finalized Part

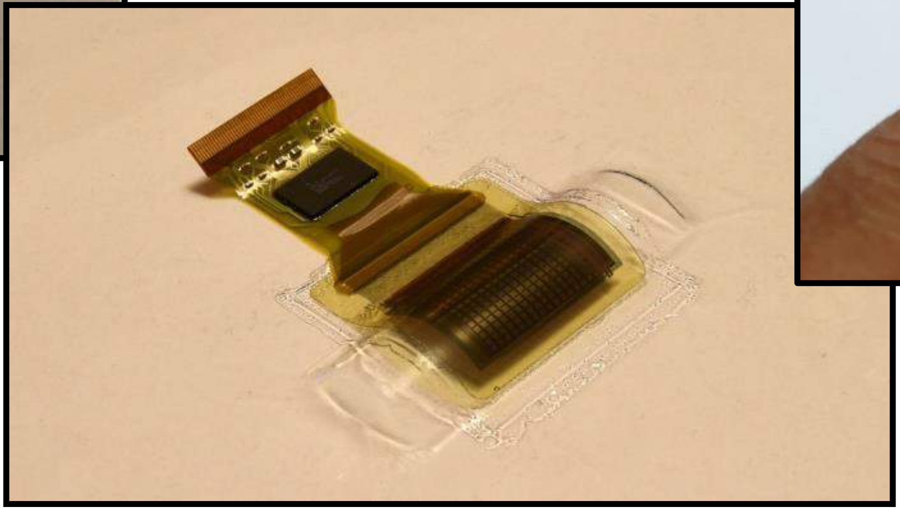
Thermoformed Imager Arrays

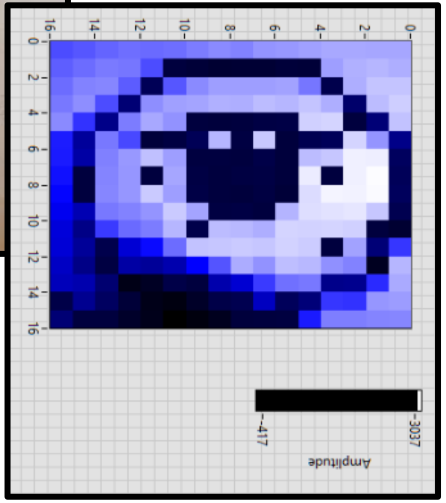
Imaging of curved sheep within 2D OPD array





OPD photodetector array on glass

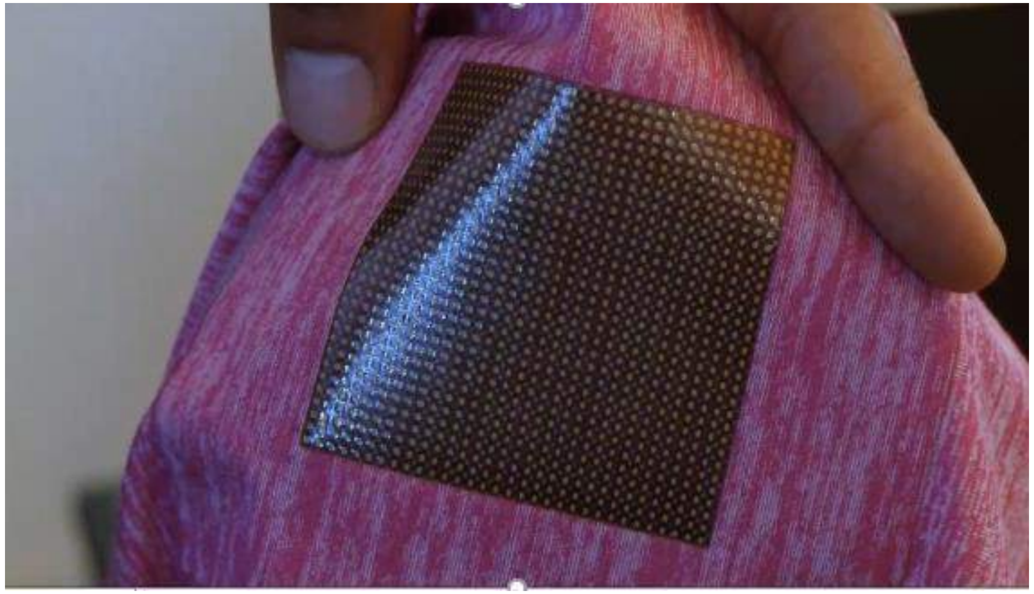




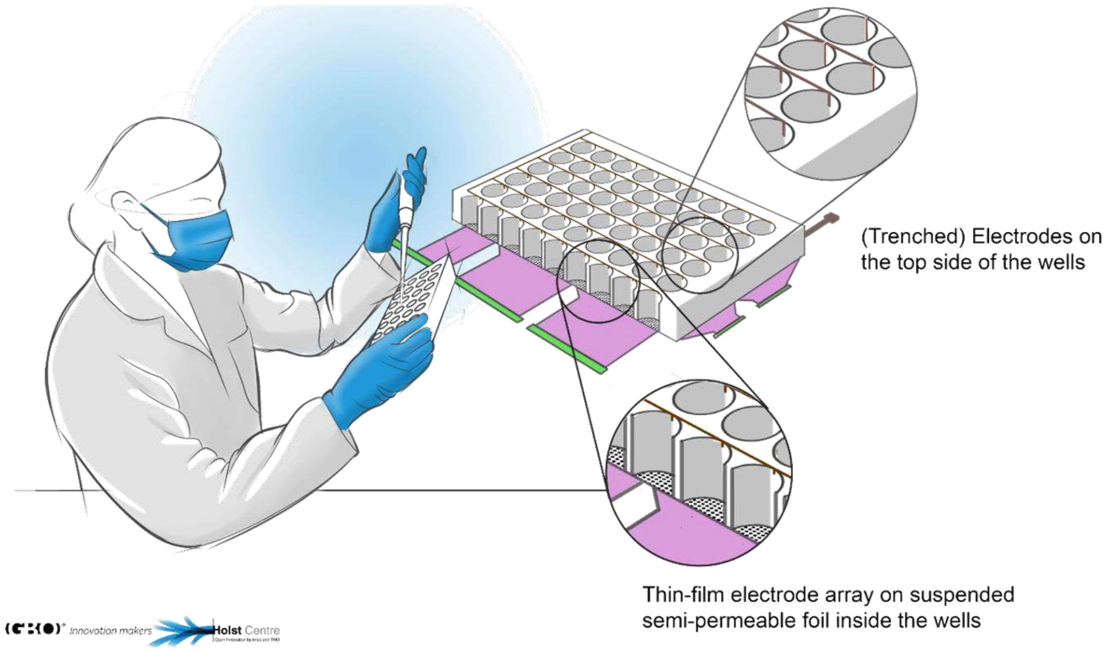
Curved thermoformed array

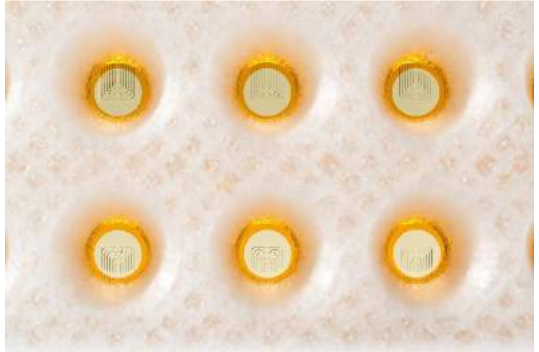
Read-out of curved sheep using 2D OPD array

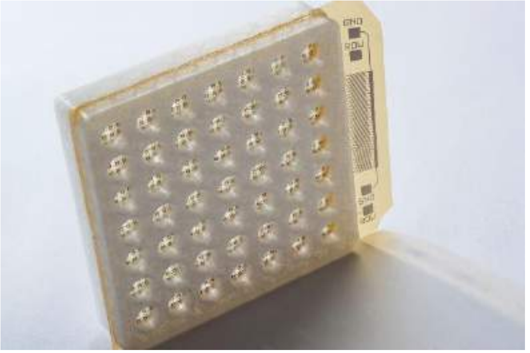
In-Textile Displays

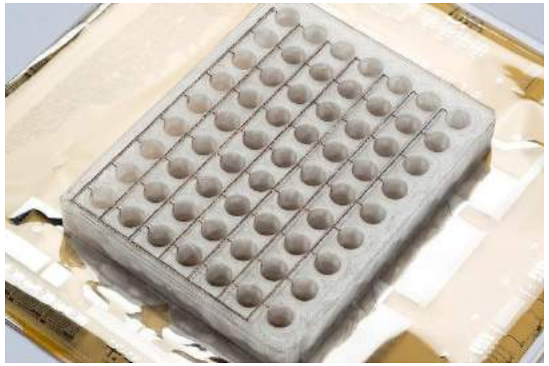


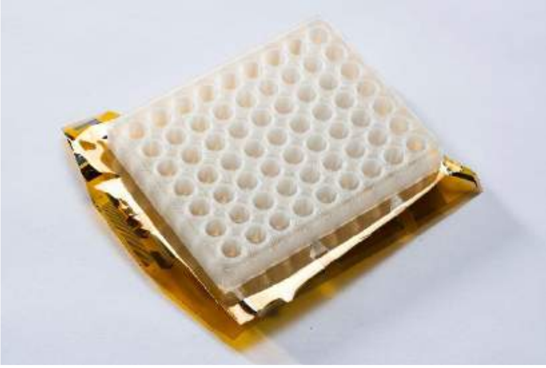
Smart Multiwell TEER Plates











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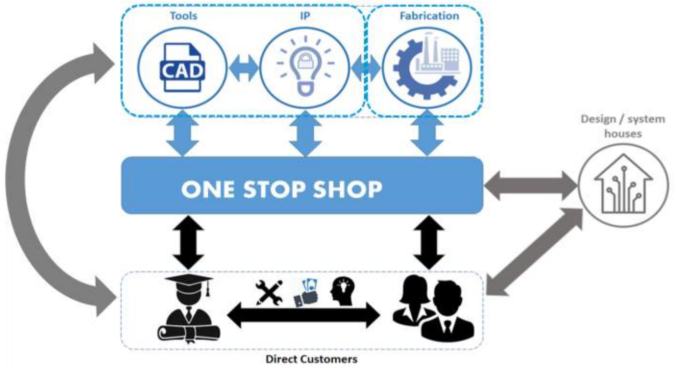
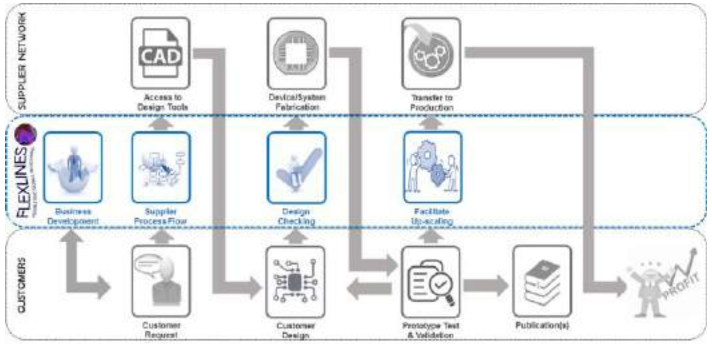
FLEXIBLE ELECTRONICS PROTOTYPING

- One-Stop-Shop

  Partnership Cooperation Model

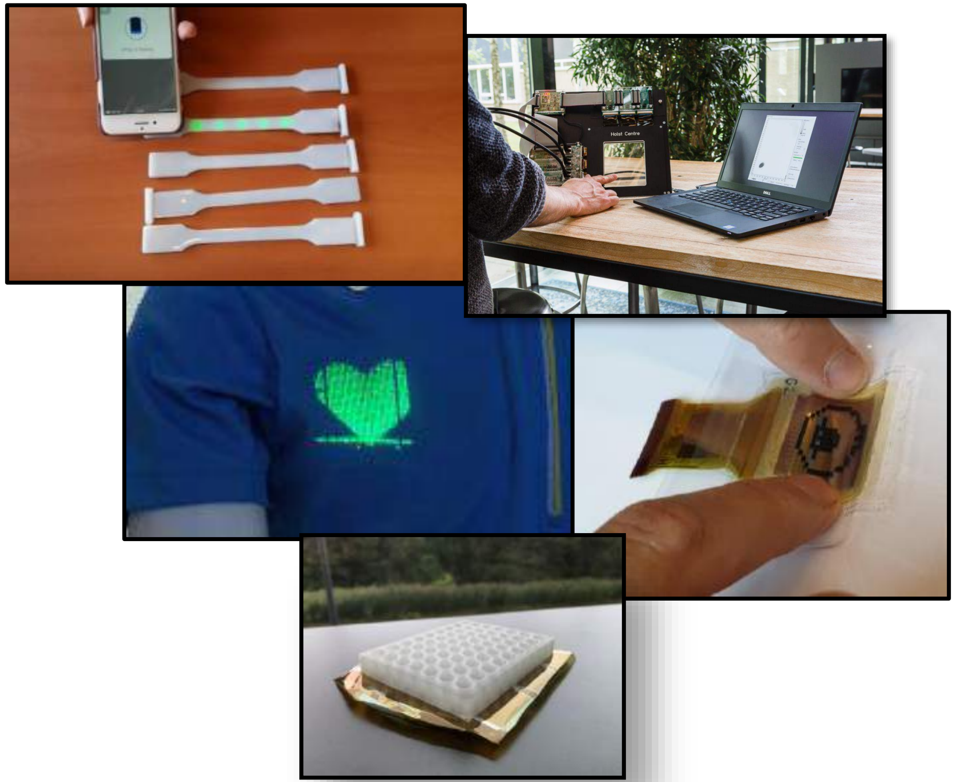




- Core Offer

  Design & Realization Multi-project FPD Sheets Electronics-on-Foil

- Optional Offer
  - Various Integration Technologies



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Europees Fonds voor Regionale Ontwikkeling

Thank you!

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Voor ieder van ons

Provincie Noord-Brabant

provincie limburg

gesubsidieerd door de Provincie Limburg

SMART HUB

VLAAMS-BRABANT

Understanding and Improving TFT Performance

René Janssen, Wentao Huang & Tamer Dogan
Eindhoven University of Technology

Main results

New infrastructure

- Set-up for photothermal deflection spectroscopy (PDS) measurements
- Set-up for sub-band gap photocurrent measurements
- Automated set-ups for variable temperature semiconductor characterization

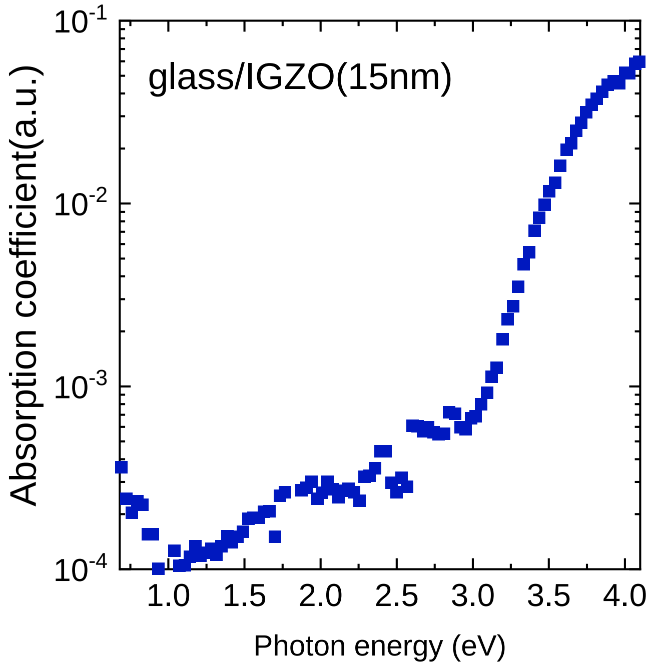
New achievements

Aim: Enhance current drive/switching rate by enhancing mobility or reducing channel length

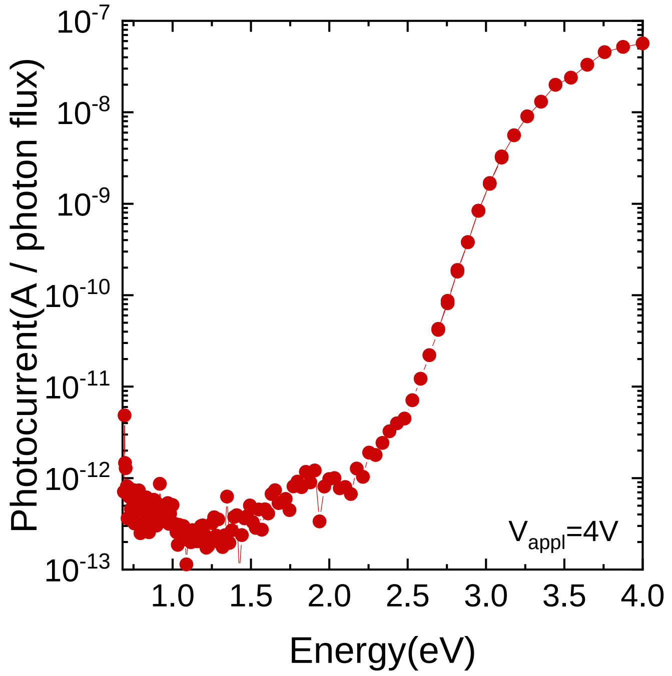
- Indium-gallium-zinc oxide (IGZO) thin film transistors with ultra thin (< 10 nm) layers
- 1000-Pixels per inch transistor arrays using multi-level imprint lithography

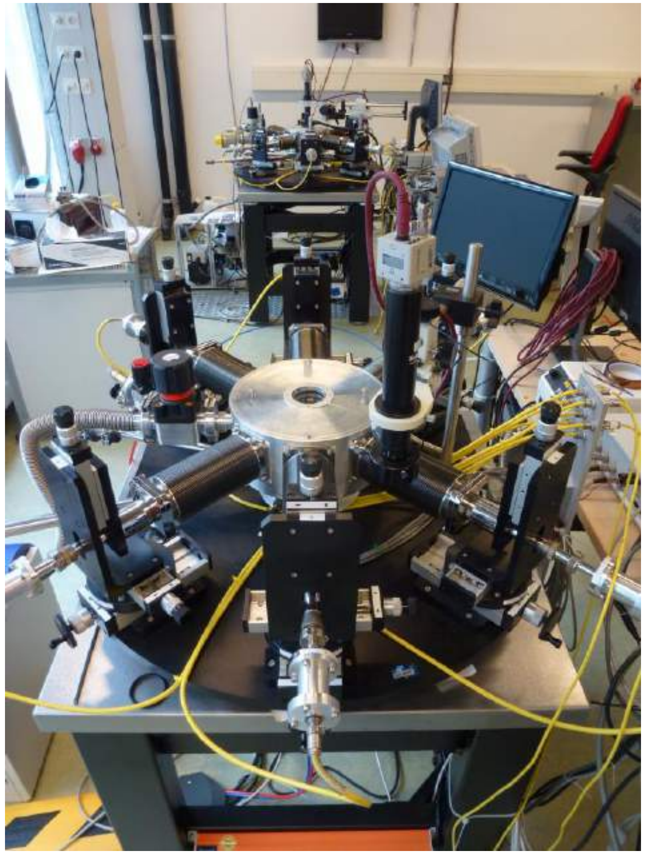
Infrastructure

PDS
IGZO sub-gap states



Photocurrent
IGZO sub-gap states





Atomic layer deposition of indium-gallium-zinc oxide

Amorphous **IGZO** is widely used in industry for standard backplane electronics due to its attractive properties such as high electron mobility/good uniformity/low leakage current/low fabrication cost/large-area scalability

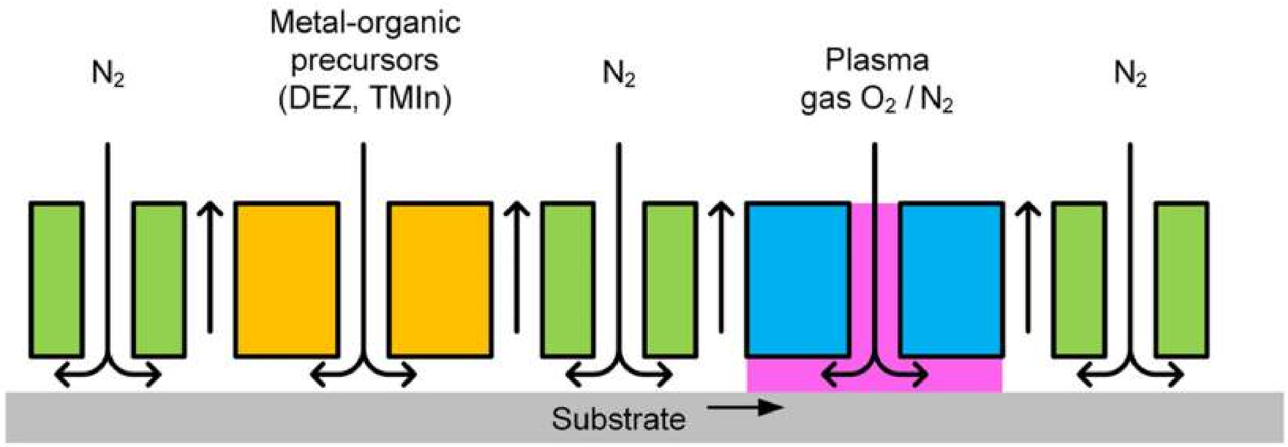
Low-dimensional IGZO is particularly of interest since devices with dimension close to the carrier accumulation layer enable a completely depleted transistor channel and could potentially overcome the intrinsic bulk mobility limitation

Therefore, **atomic layer deposition**, rather than the most widely-used sputtering technique, is investigated in IGZO film fabrication as the former could provide more precise control of film composition and thickness

Spatial atomic layer deposition

Atomic layer deposition (ALD) is a gas phase deposition technique which enables digital control of film thickness and composition with excellent conformality on nonplanar surfaces.

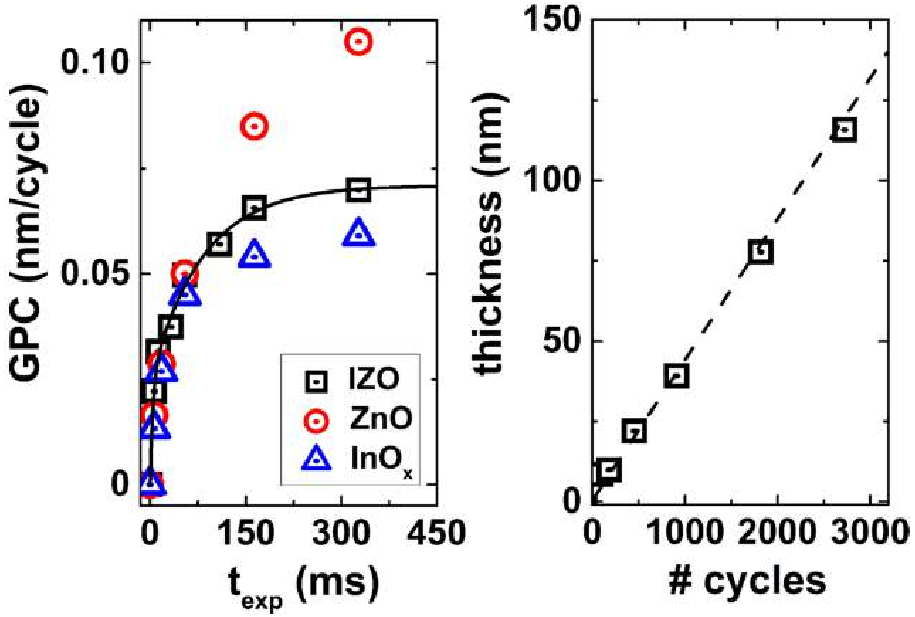
In spatial ALD (**s-ALD**) different precursor injection and reaction steps are separated spatially instead of temporally so that the requirement of time-consuming purge steps can be eliminated.



A schematic of the spatial ALD concept

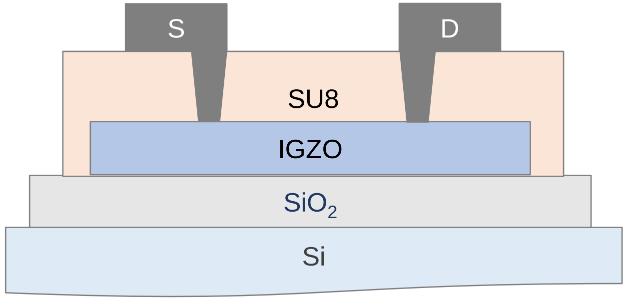
Spatial atomic layer deposition

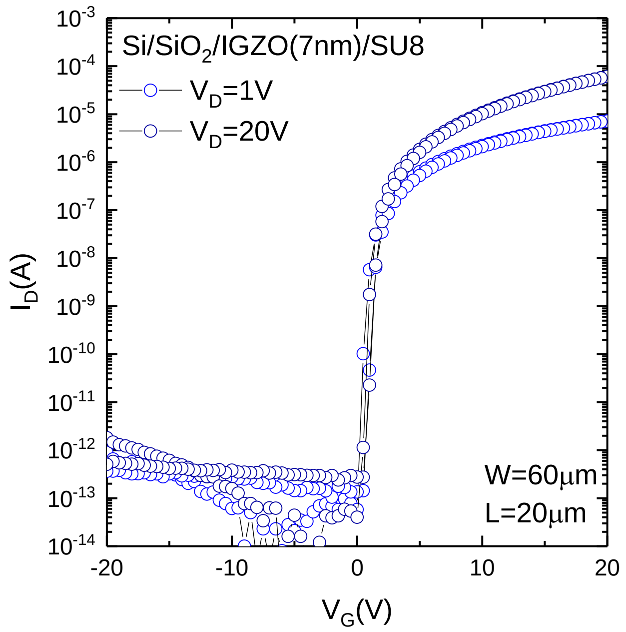
Metal precursors (DEZ, TMI, TEG) are pre-mixed before injection and plasma source is used to enable the growth of oxide at low temperature and short exposure times to the oxygen precursor.

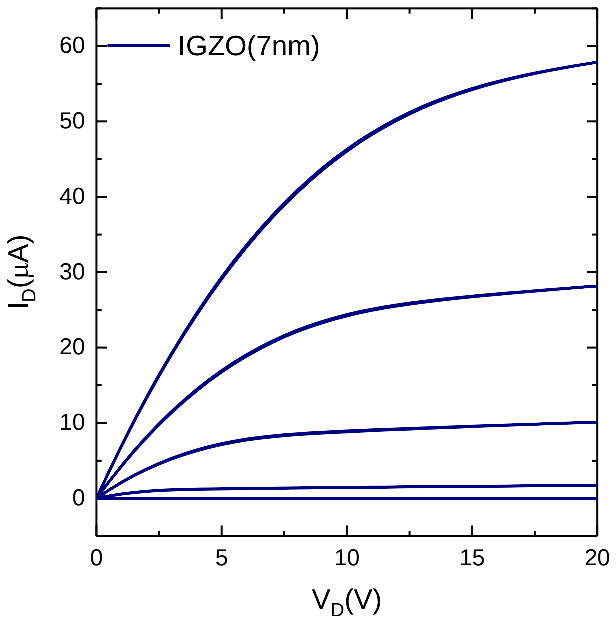


Growth per cycle (GPC) vs exposure time & thickness vs number of cycles

Electrical characterisation of IGZO TFTs by s-ALD







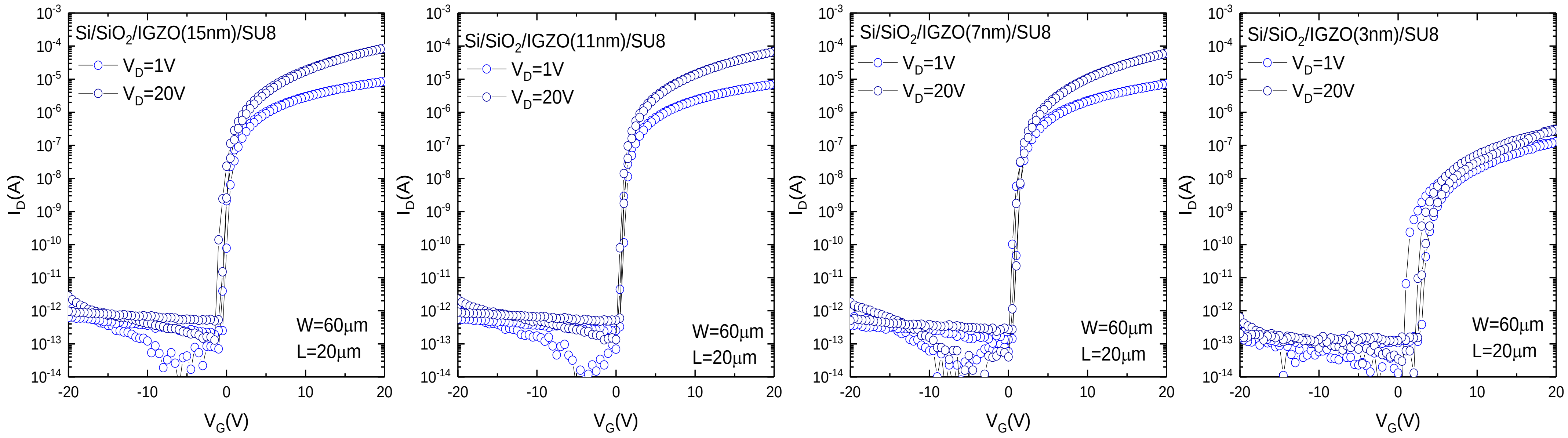
IGZO thin film transistors(TFTs) are fabricated in a bottom-gate top-contact(BG-TC) architecture with photoresist SU8 as the etch stop layer (ESL).

The transfer curves of the transistor exhibit good operating and hysteresis-free characteristics with a high electron mobility of ~10 cm^2/Vs.

The output curve of the same transistor shows excellent output characteristics with a steep rise in the low V_D region.

Thickness scaling of IGZO TFTs

The TFT measurement indicates no effect on charge transport for IGZO thickness from 15 nm to 7 nm, but a formation of degenerate transistor channel for thickness down to 3 nm.



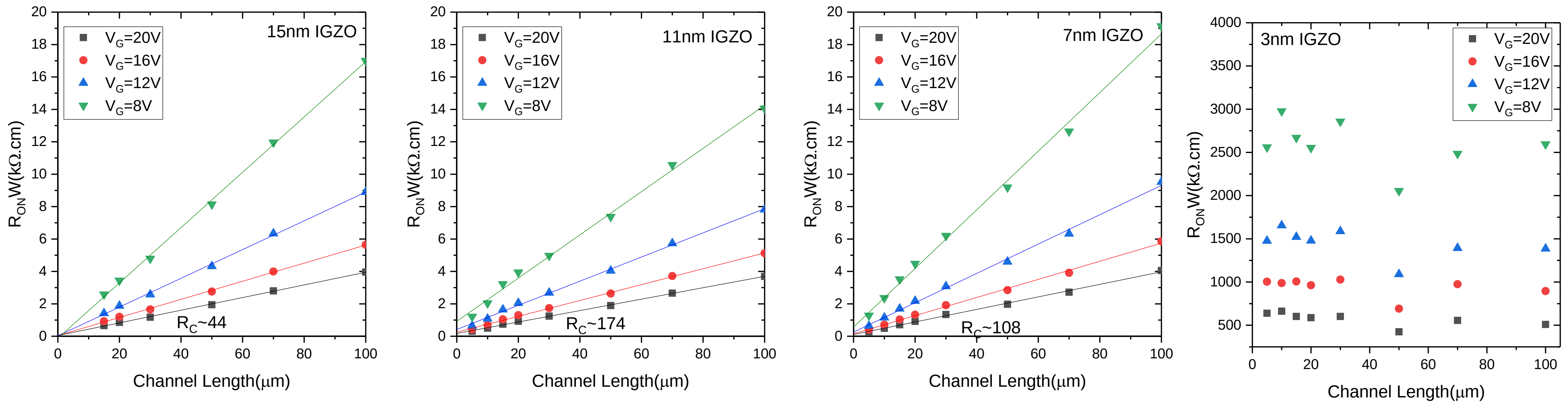
ALD cycles	200	146	93	40
Thickness (nm)	15	11	7	3
μ_{LIN}(cm²/Vs)	~11	~9	~10	~0.3

TFT R_C analysis by TLM

Contact resistance (***R*_C_**) of the IGZO TFTs is evaluated by transfer-length method (**TLM**)

TFTs with different values of L are scanned in the linear regime to extract the intercept of TLM plot, which can be used to qualify R_C. The results show very small R_C (~100 Ω·cm) for thickness from 15 to 7 nm.

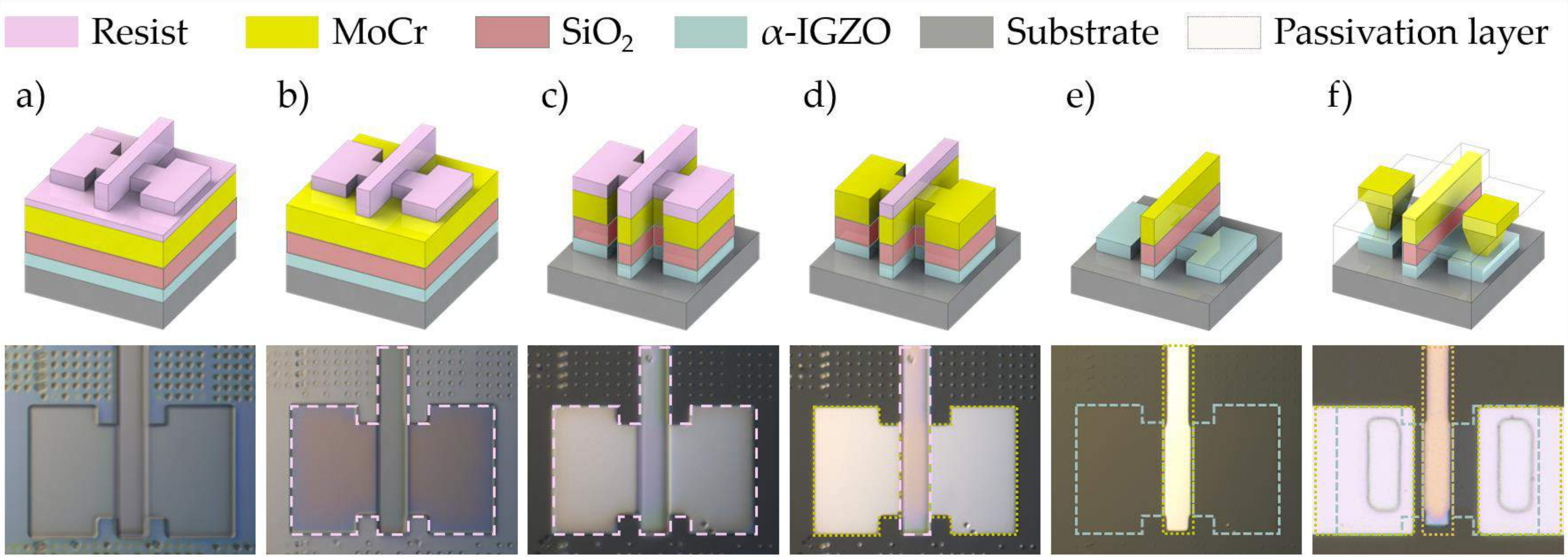
In contrast, TFT with 3 nm IGZO exhibits high R_{ON} and L independence in the TLM plot, indicating that the 3 nm IGZO device suffers from large R_C



Substrate conformal imprint lithography

- Need for high-resolution cost-effective methods to fabricate TFTs over large areas
- Photolithography can deliver line/space patterning resolution of 1-2 µm
- Multi-level imprint lithography potentially combines precision patterning with large-area cost effectiveness
- Employ substrate conformal imprint lithography (SCIL) to realize IGZO TFTs with sub-micrometer channel length in high-density arrays.

TFT fabrication via multilevel imprint lithography



Resist structure height differences of 0.5 µm in 3D.

Reactive ion etching of residual resist

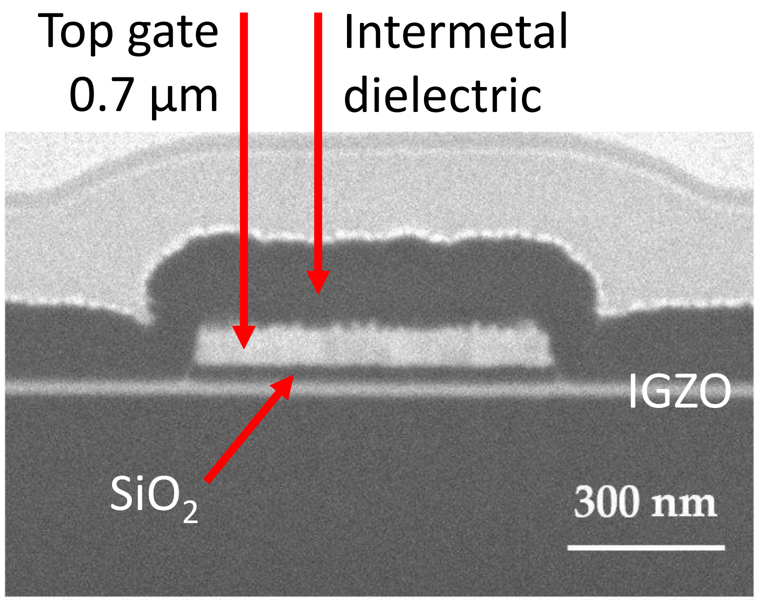
Wet and dry etching

Reactive ion etching

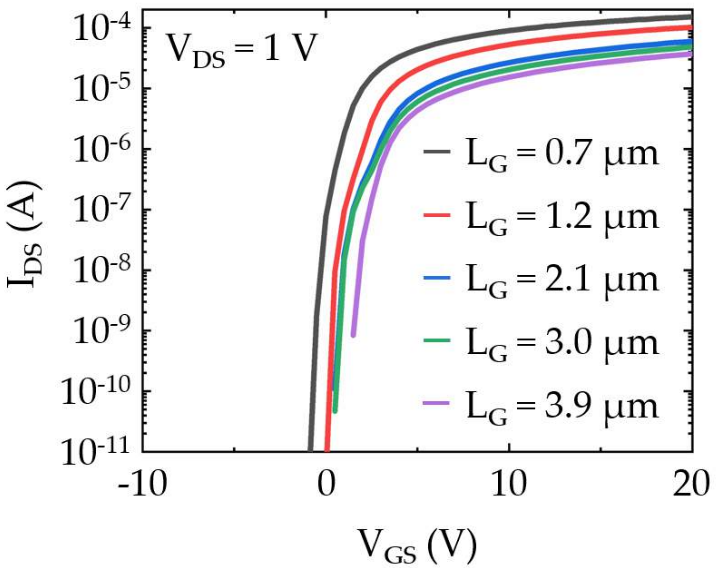
Removal of gate metal & insulator, Doping of exposed IGZO

Metallization of source and drain contacts

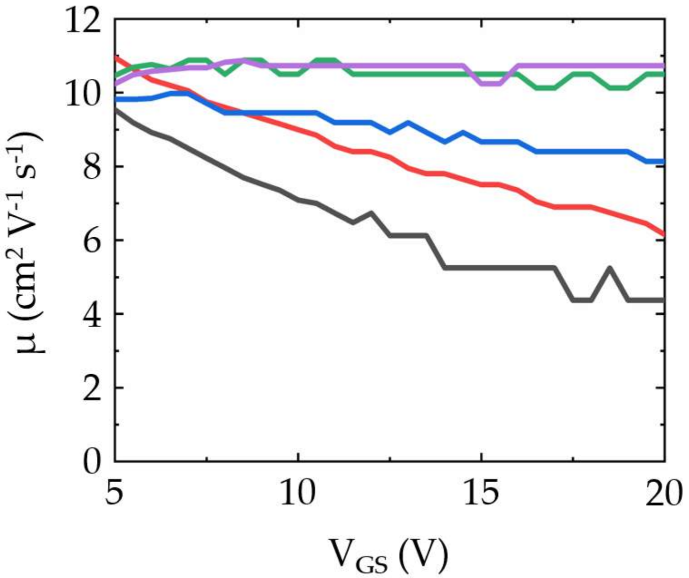
α-IGZO TFT characteristics



SEM cross-section of TFT with minimum channel length L = 0.7 µm.

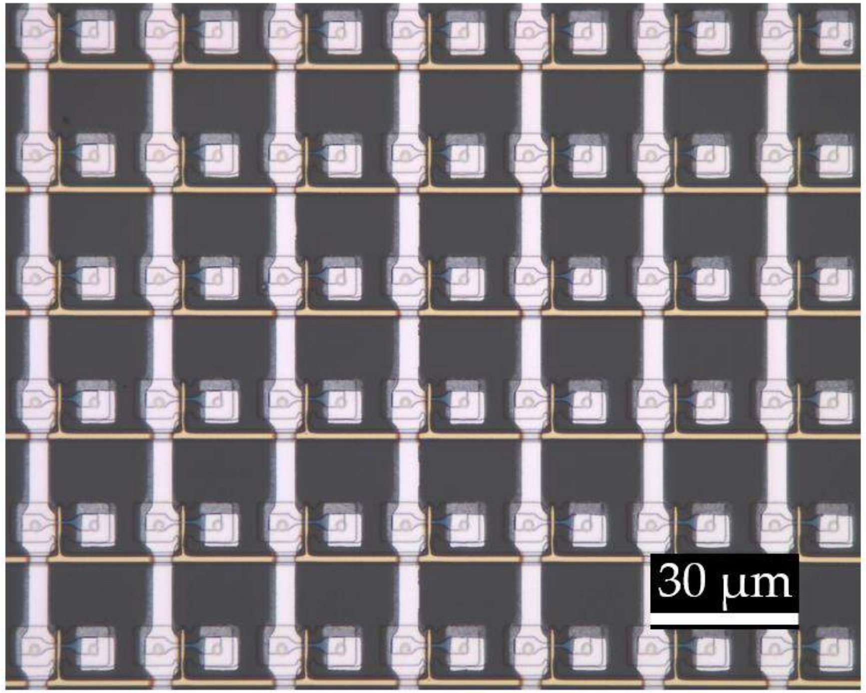


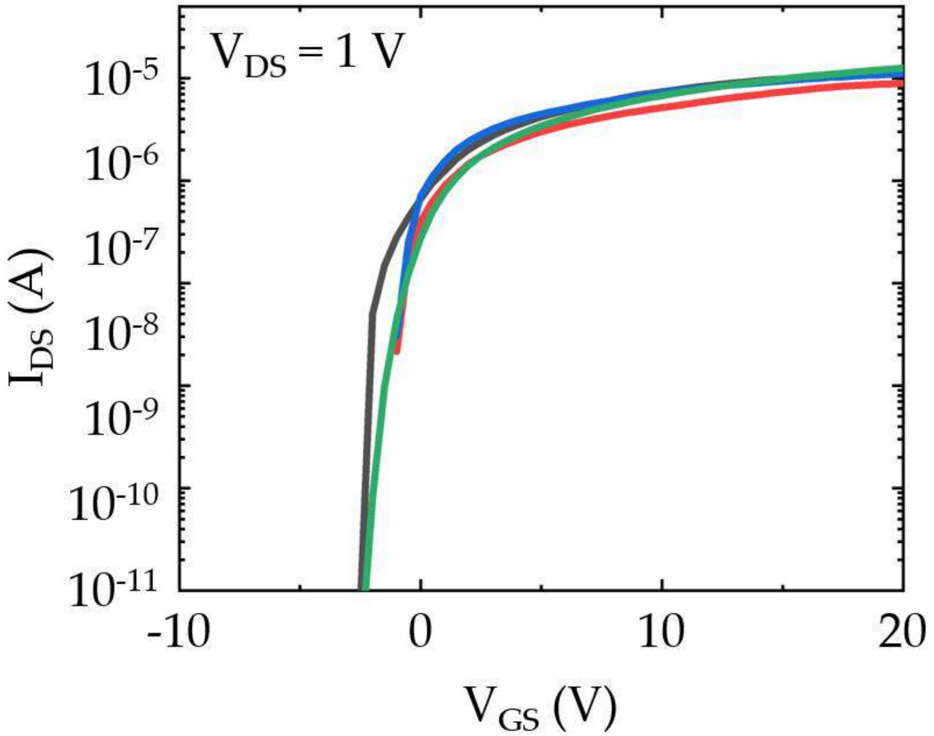
Transfer curves
L = 0.7 – 3.9 µm



Mobility
L = 0.7 – 3.9 µm

1000 ppi α-IGZO backplane array of 0.8 µm TFTs





T. Dogan, *IEEE Electron Device Lett*. **2020**, *8*, 1217−1220.

Typical transfer curves of α-IGZO TFTs (W/L = 1.2/0.8 µm) in the array.

Conclusions

- IGZO films by s-ALD fabricated and characterized in TFT architecture. The results benchmark the performance of s-ALD IGZO TFTs fabricated in ESL architecture.
- Thickness scaling experiment was performed to explore the feasibility of low-dimensional IGZO TFT by s-ALD.
- Functional IGZO device with thickness down to 7 nm, but device with 3 nm exhibits a considerably large R_C. Possibly related to roughness dielectric or kick start ALD growth
- 1000 ppi TFT backplane arrays with sub-micrometer α-IGZO top-gate self-aligned thin-film transistors using multi-level imprint lithography down to channel lengths of ~700 nm.
- The α-IGZO transistors switch on close to 0 V and have mobility ~10 $cm^2\ V^{-1}\ s^{-1}$, similar to photolithography-benchmark devices.

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Provincie Noord-Brabant
provincie limburg gesubsidieerd door de Provincie Limburg
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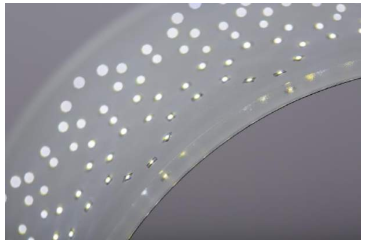
Flexlines project WP5: Integrate flexible electronics with engineering thermoplastics by injection over-molding

Adri van der Waal, Bart Peeters, Albert van Breemen, Auke Kronemeijer, Margreet de Kok

10TH dec 2020 Flexlines closing event: webinar

TNO / Holst Centre



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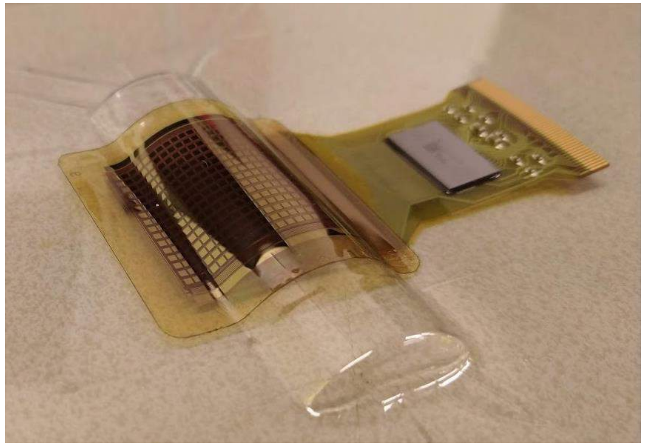
Hybrid printed electronics for integration

- Background of challenges for electronics in thermoforming and injection moulding

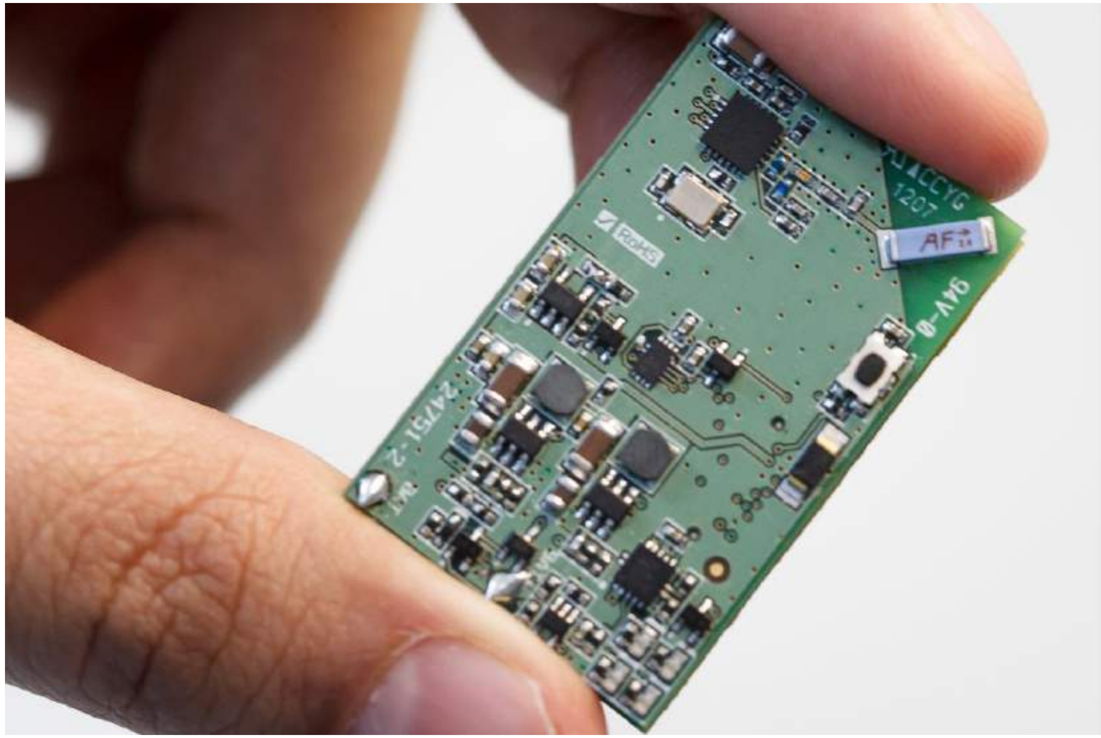
- Two examples of technology developed in pilot line:

  - 1. Overmoulded hybrid printed electronics
  - 2. Thermoformed hybrid electronics



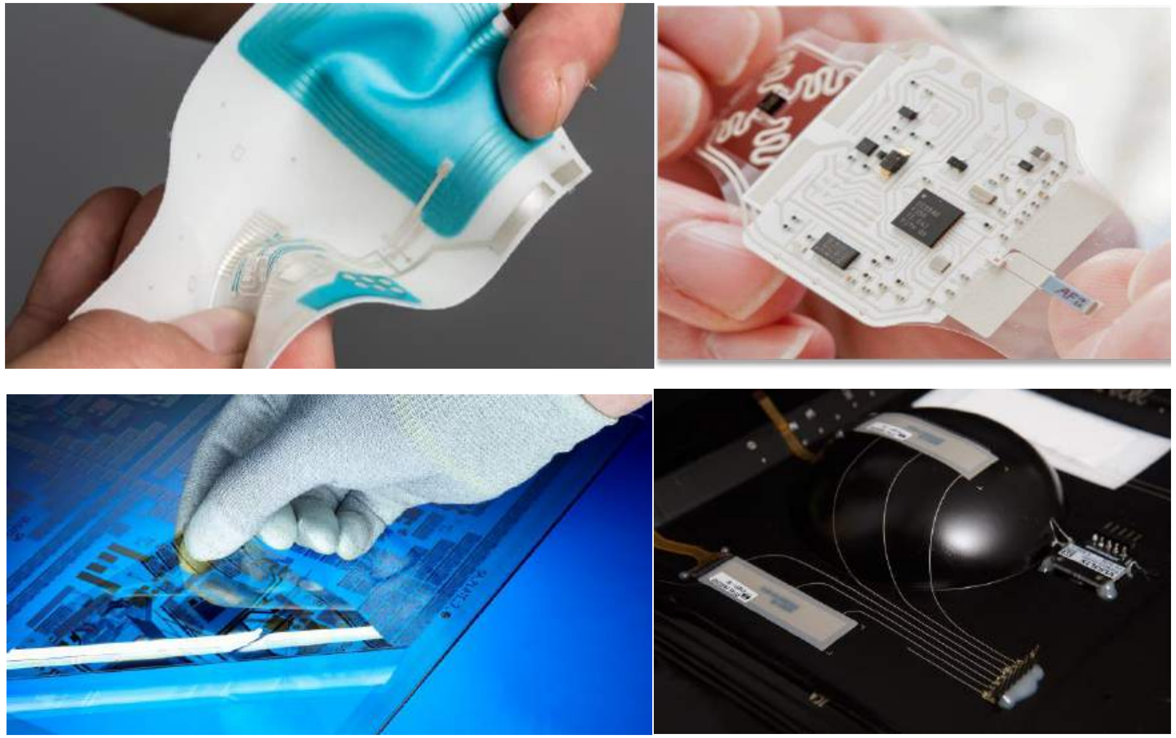
TNO at Holst Centre: freeform electronics by printed electronics

electronics today



- **Limited formfactor** - *rigid*

electronics tomorrow



- **New formfactors** - *flexible, stretchable, structural*

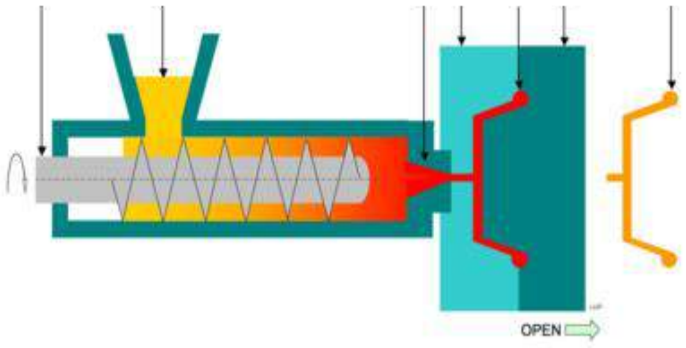
Hybrid printed electronics

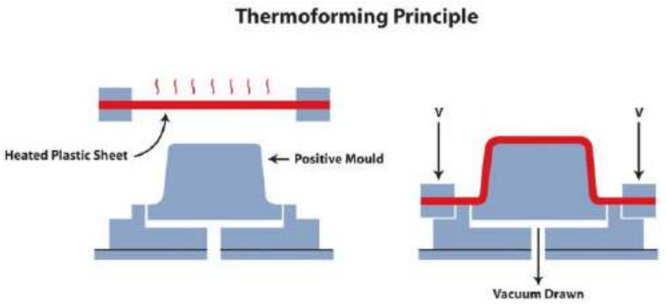
Roll-2-roll screen printing

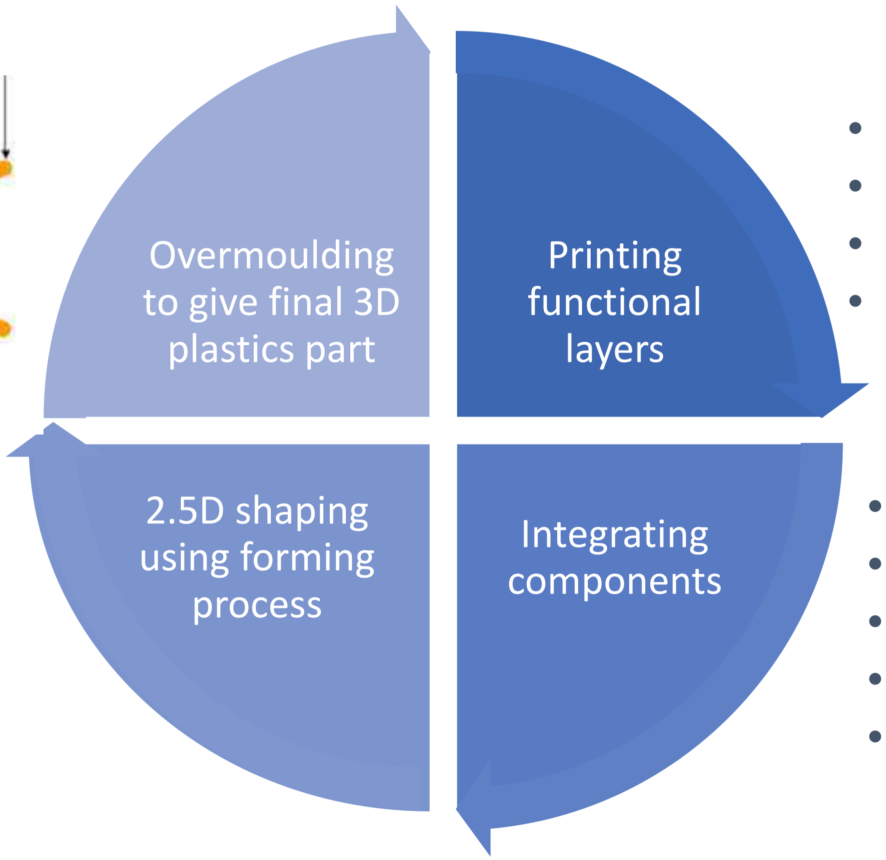
Roll-2-roll component assembly

High Pressure Thermoforming

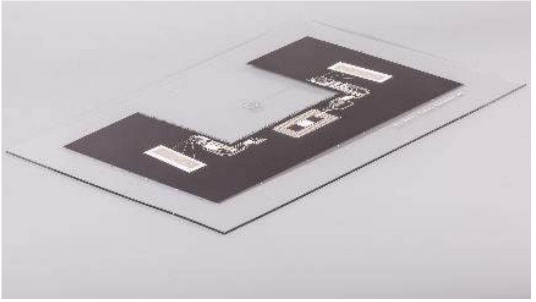
Development of structural electronics



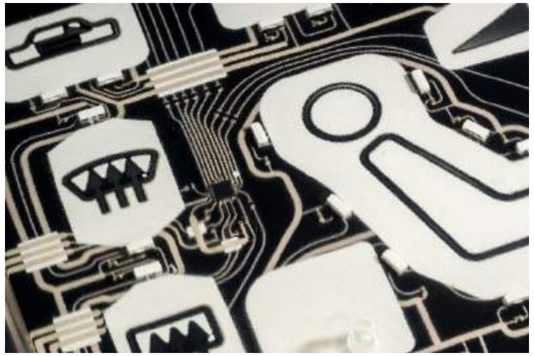




- substrates
- graphics
- electronic circuit
- sensors (e.g. touch)



- chips
- LEDs
- displays
- adhesives
- lamination

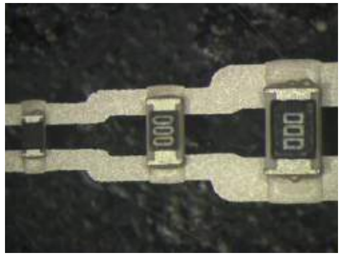


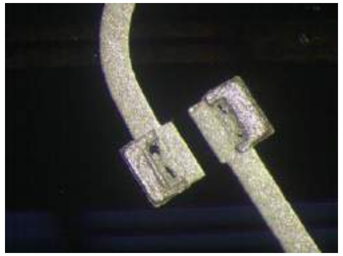
All process steps are strongly inter-linked…

Challenges for integration

Thermoforming
- Temperature (160 °C for PC)
- Pressure (60 – 100 Bar)
- Deformation

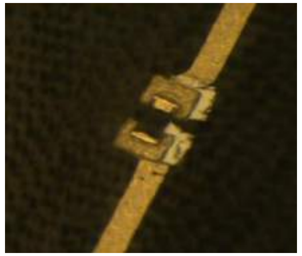
Resulting in:
- Disconnection of components
- Thermal shock and damage to electronics

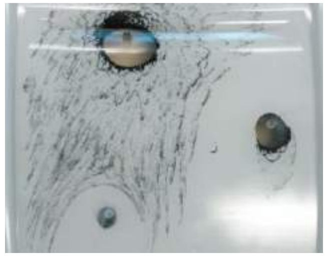




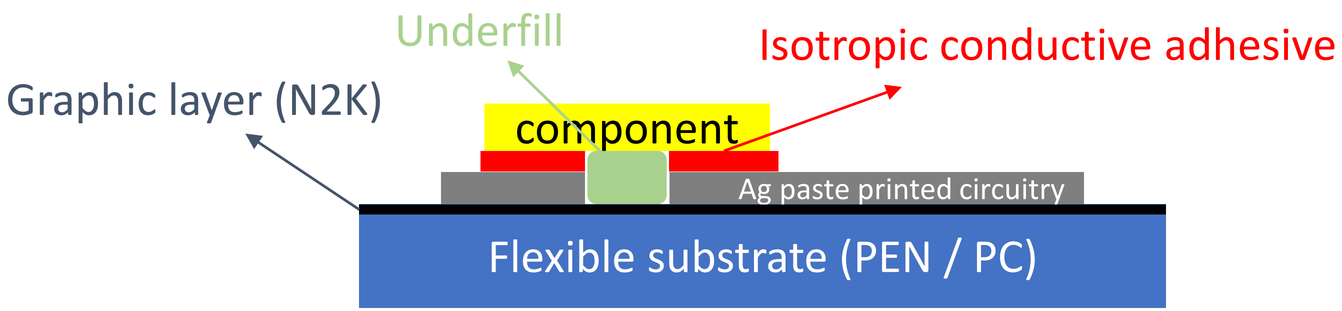
Injection moulding
- Temperature (260 °C for PC-resin)
- Pressure (<200 Bar)

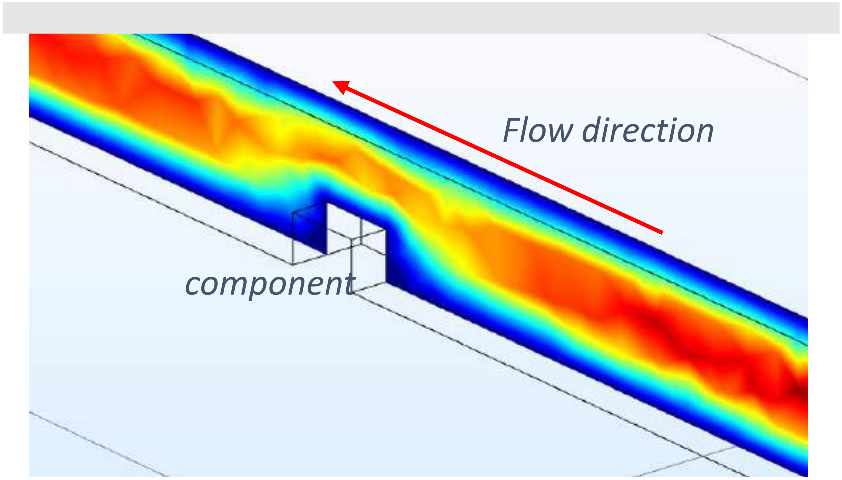
Resulting in:
- Disconnection of components
- Thermal shock and damage to electronics
- Wash-out of graphics and electronic tracks





Example 1:
Overmoulded hybrid printed electronics:





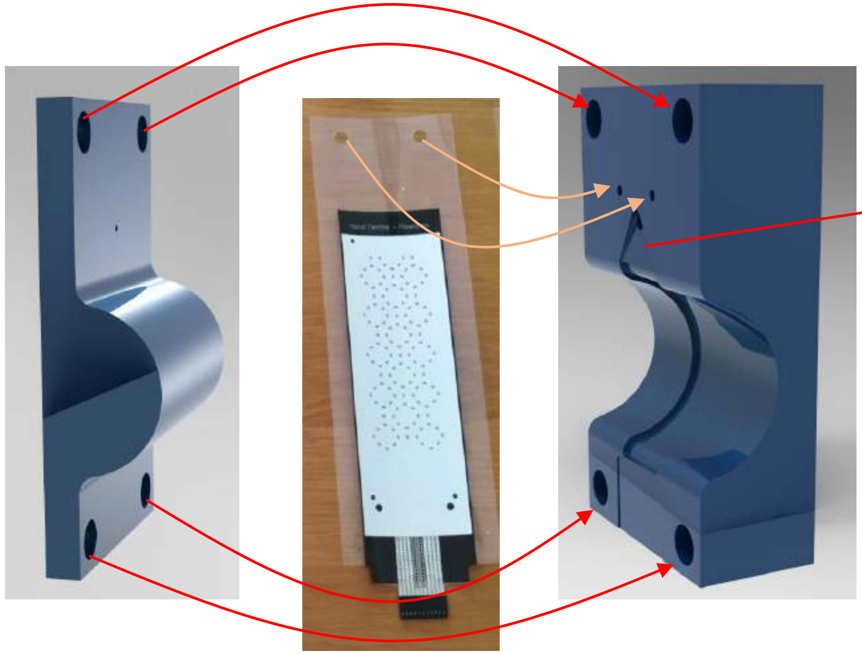
Fluid velocity distribution in mold

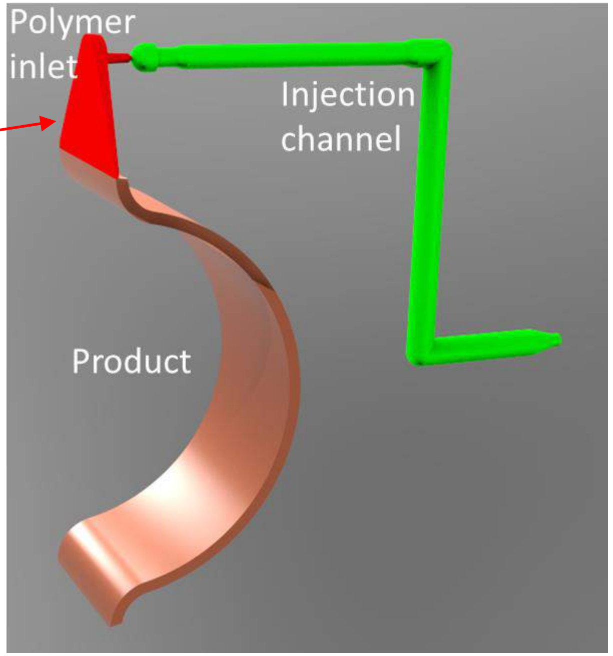
- Washout of graphics
- Washout and disconnection of electronics
- Adhesion between layers
- Wrinkles in injection moulded part

Integration by injection moulding

Overmoulding is performed with a semi-circular mould, designed by BMC – TNO.

In this mould, the flexible substrate is bent in one direction





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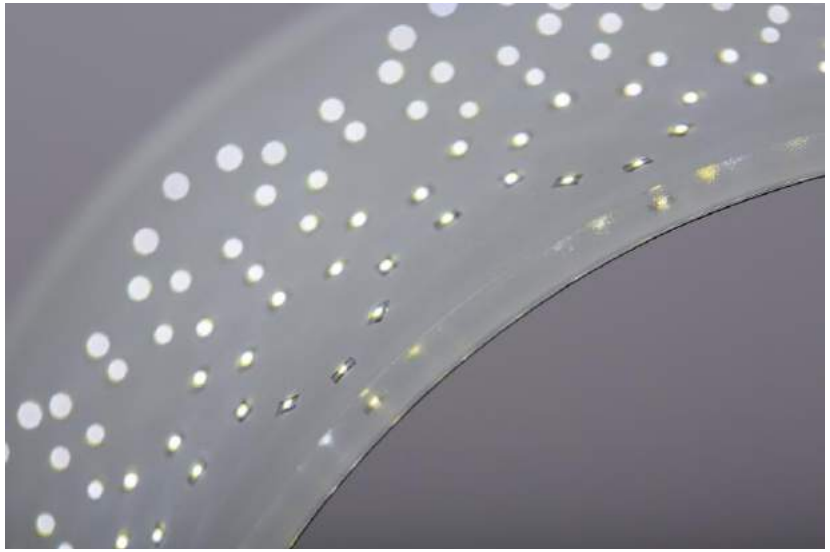
Functional demonstrator

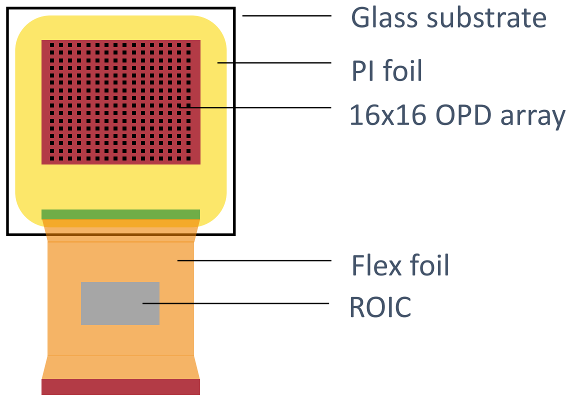


Functionalities:

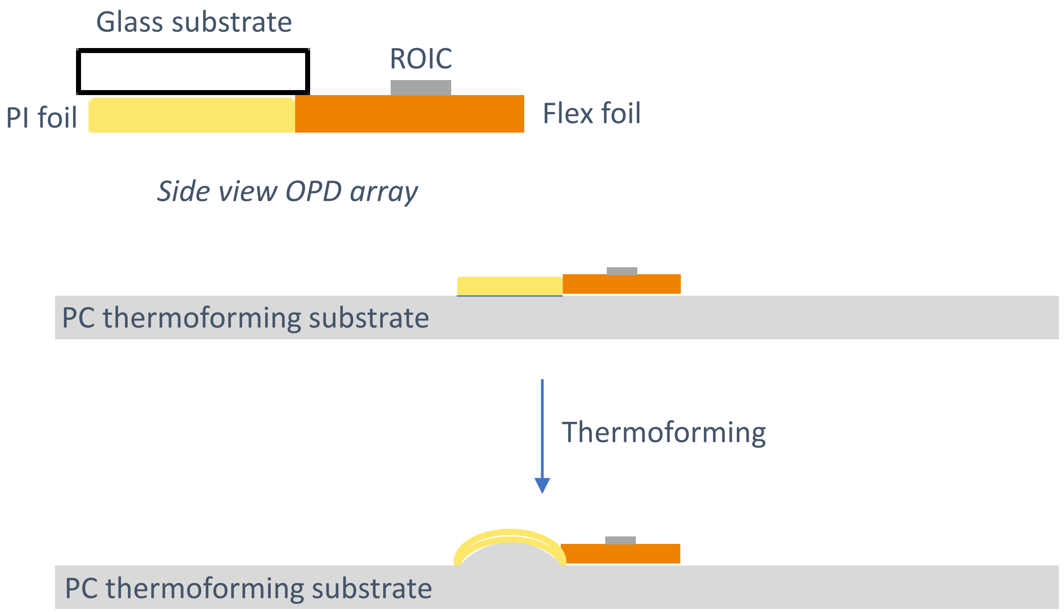
- Capacitive touch
- LED integration

Example 2:
Thermoformed hybrid electronics:

- Photodetector array laminated onto PC and then thermoformed
- Challenges: temperature sensitive OPD and deformation in TF process

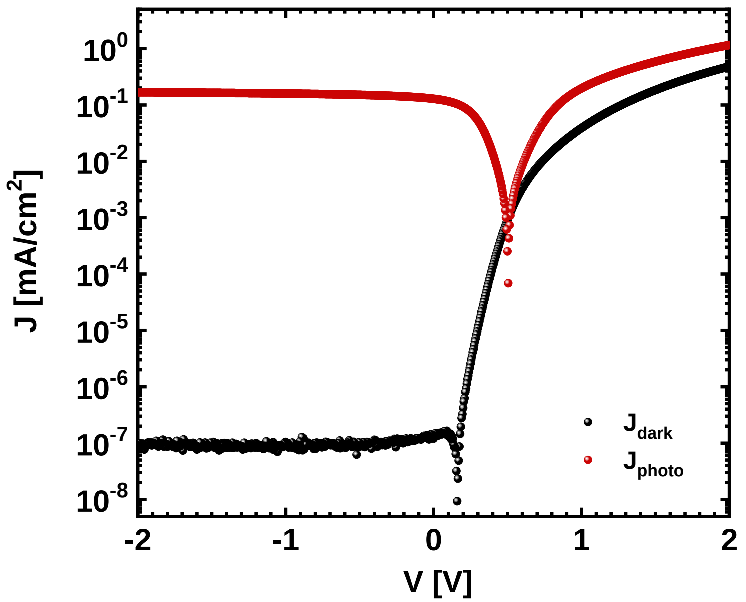


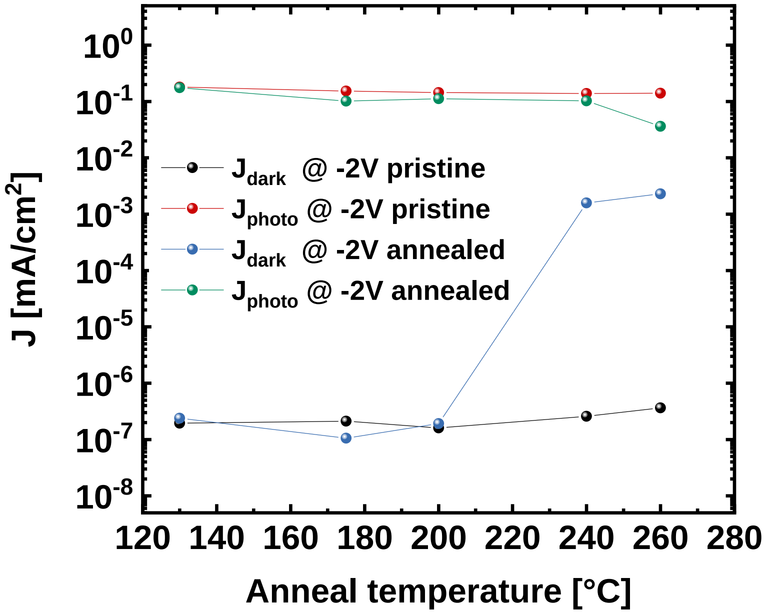
Top view OPD array

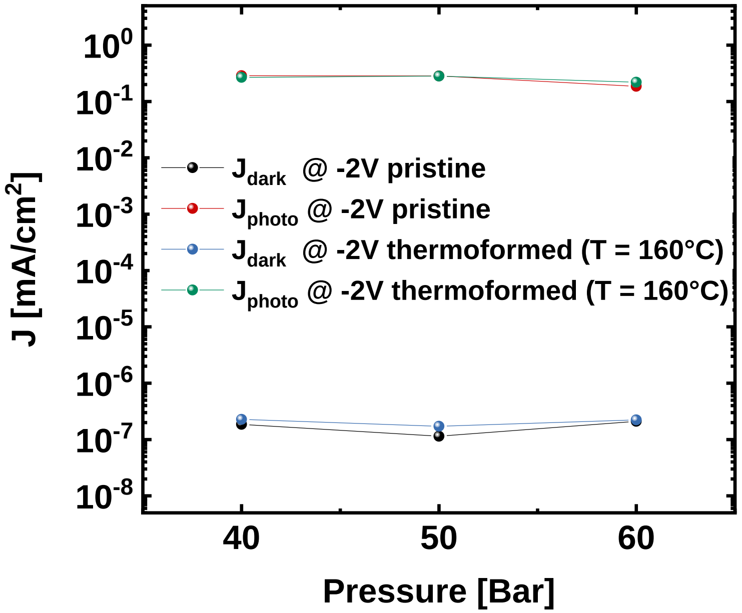


Side view OPD array

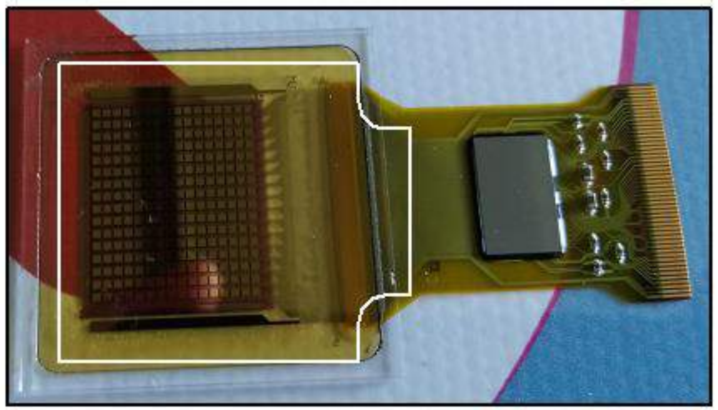
Temperature and pressure sensitivity of OPD

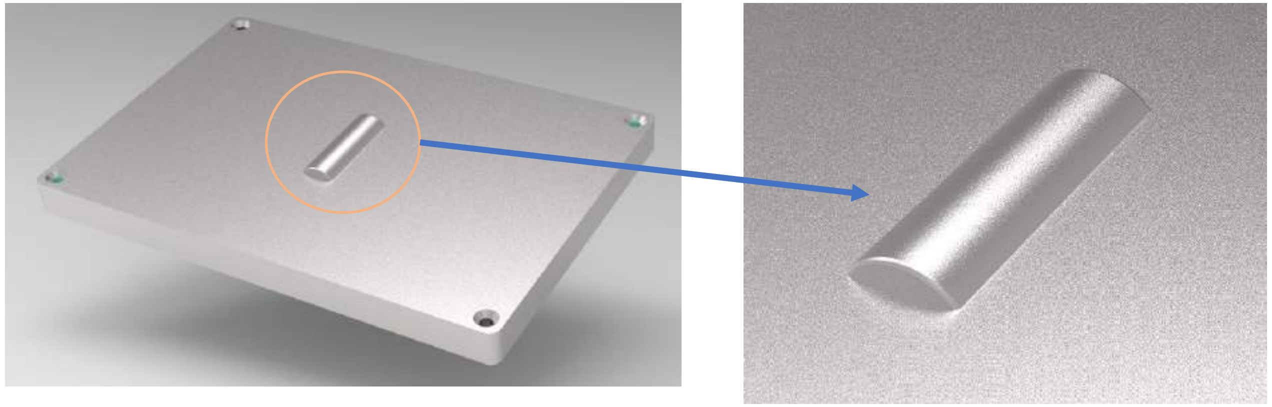


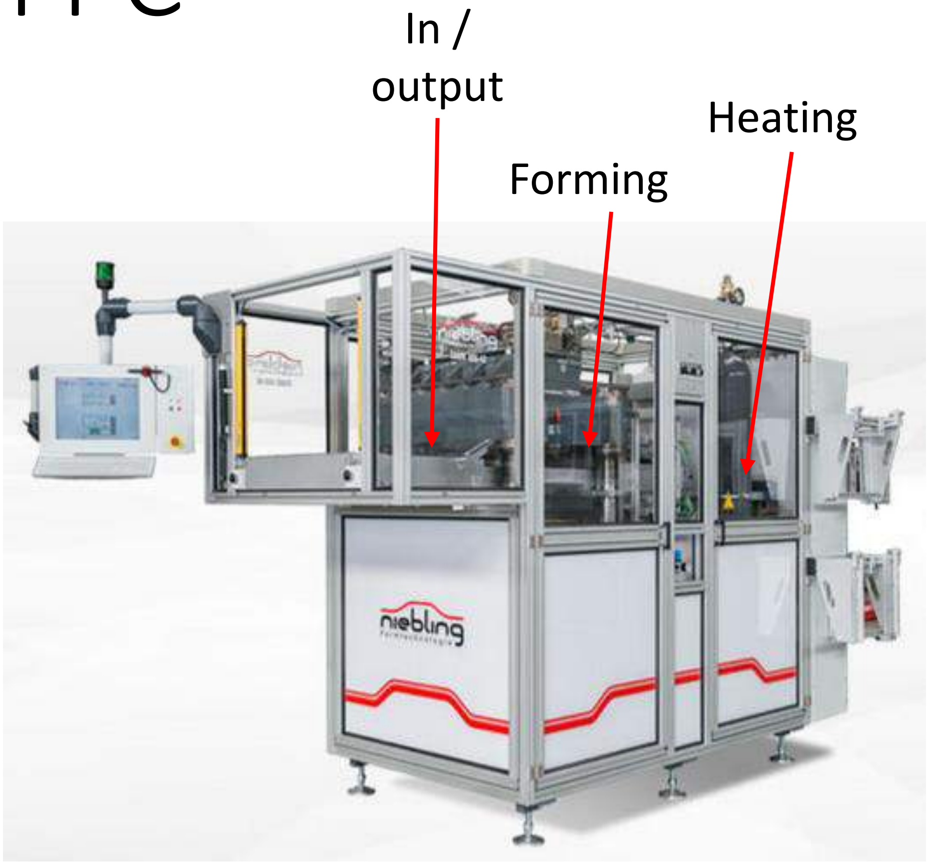




Thermoformorming of OPD on PC

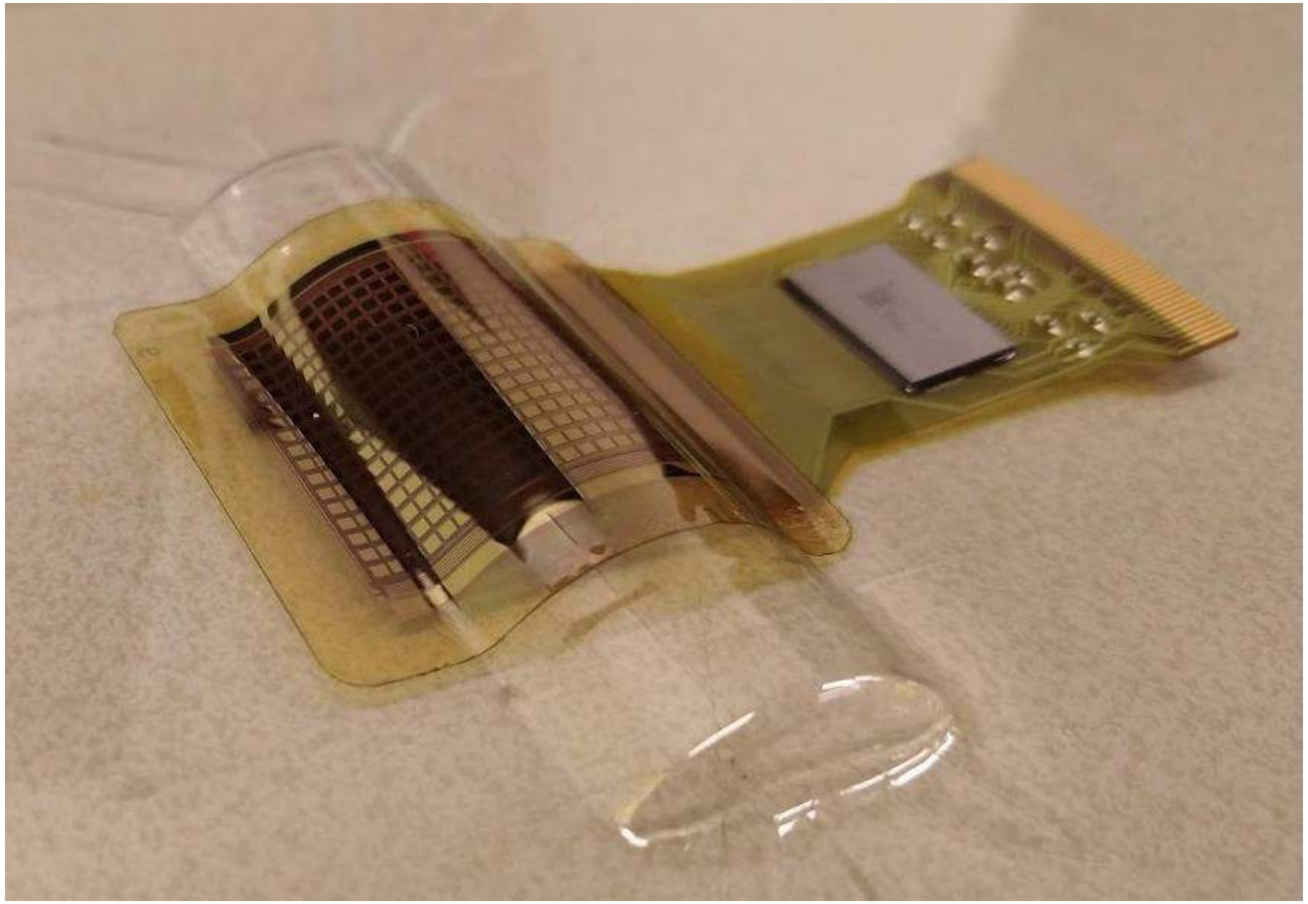






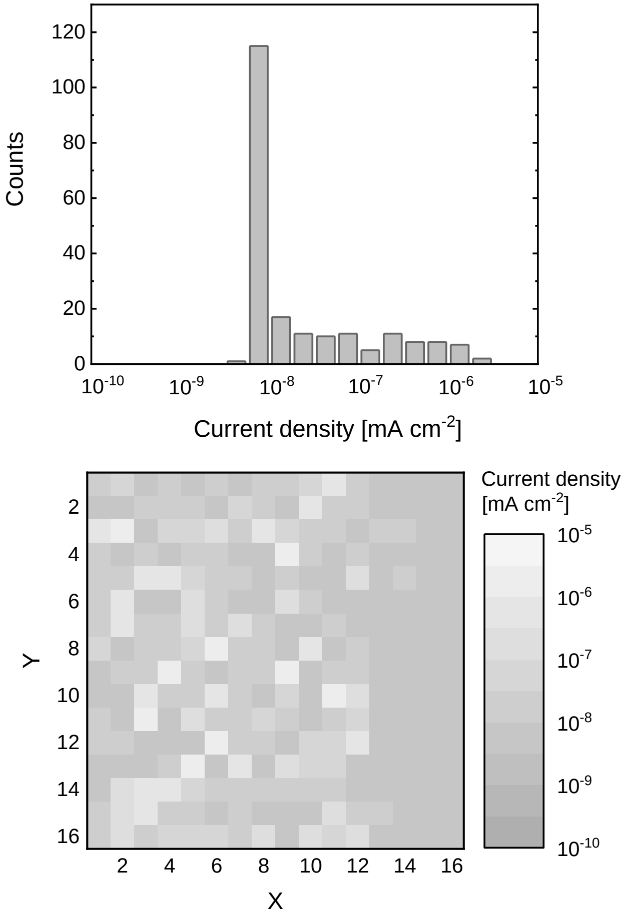
- Processing in High Pressure Forming machine (Niebling)
  - Heating time 13.5 s
  - Maximum temperature substrate (PC) 160 °C
  - Pressure 80 bar
  - Mould temperature 120 °C

16x16 OPD array after thermoforming



Characterisation of dark current

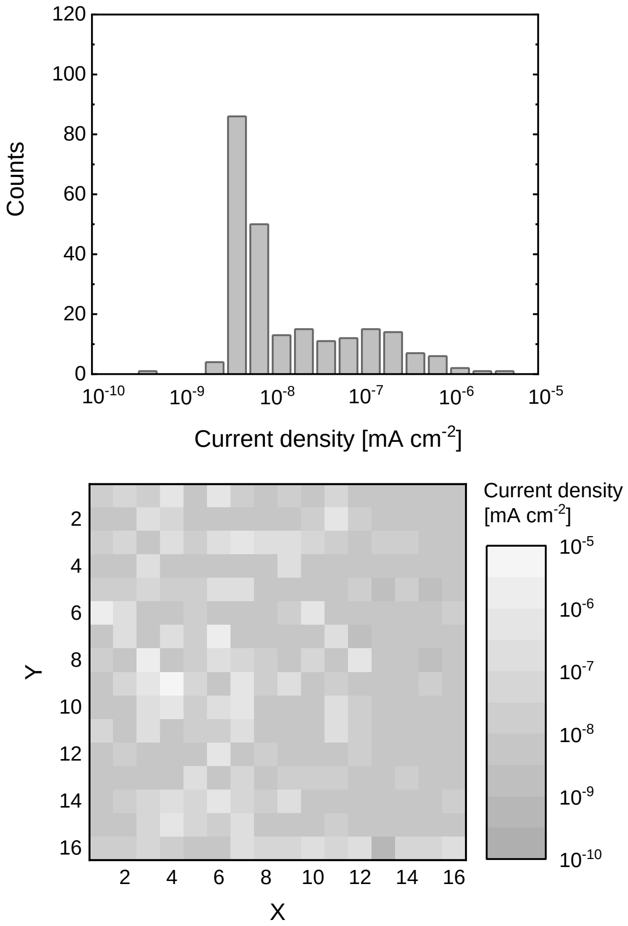
Pristine



After PC lamination

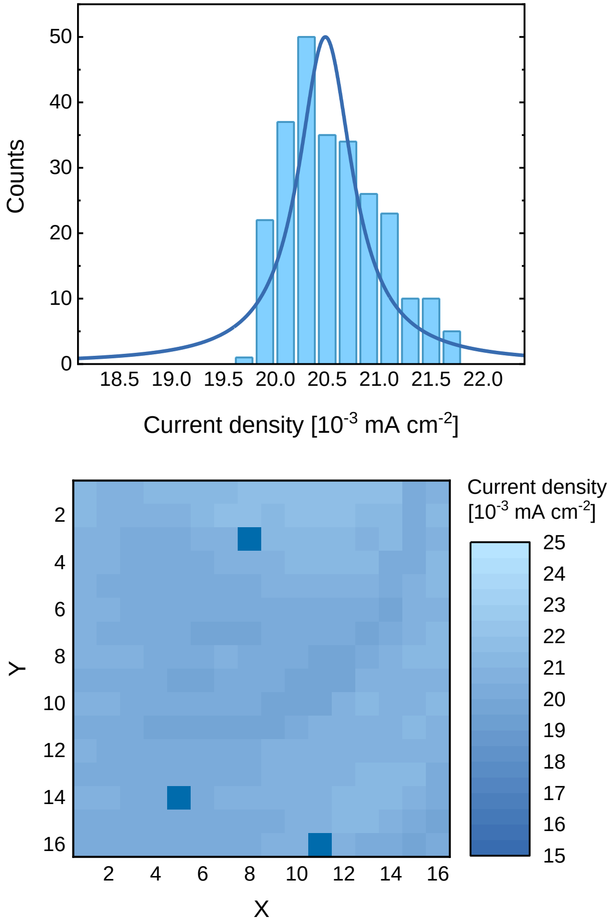
After laser delamination

After thermoform – no deform

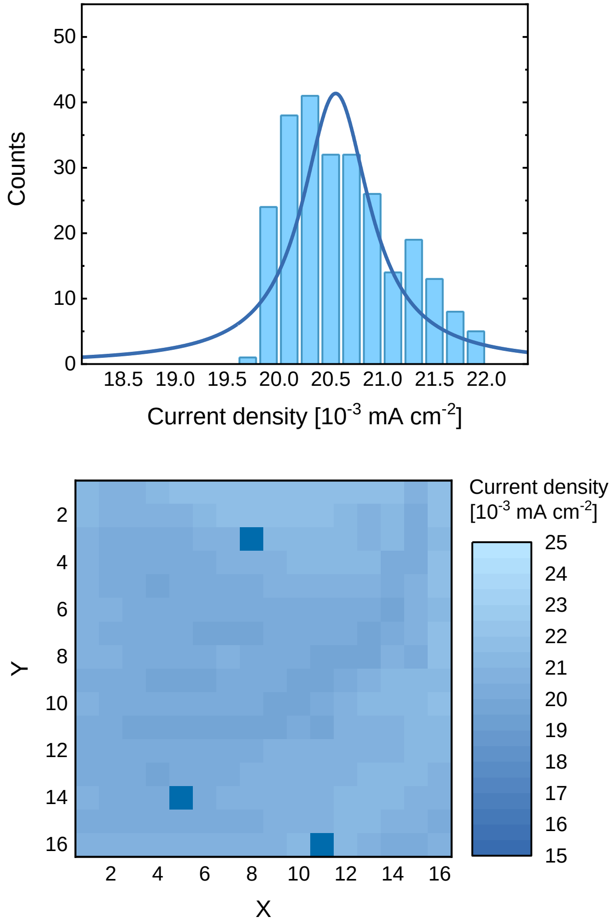


Characterisation in light (110 Cd/m^2)

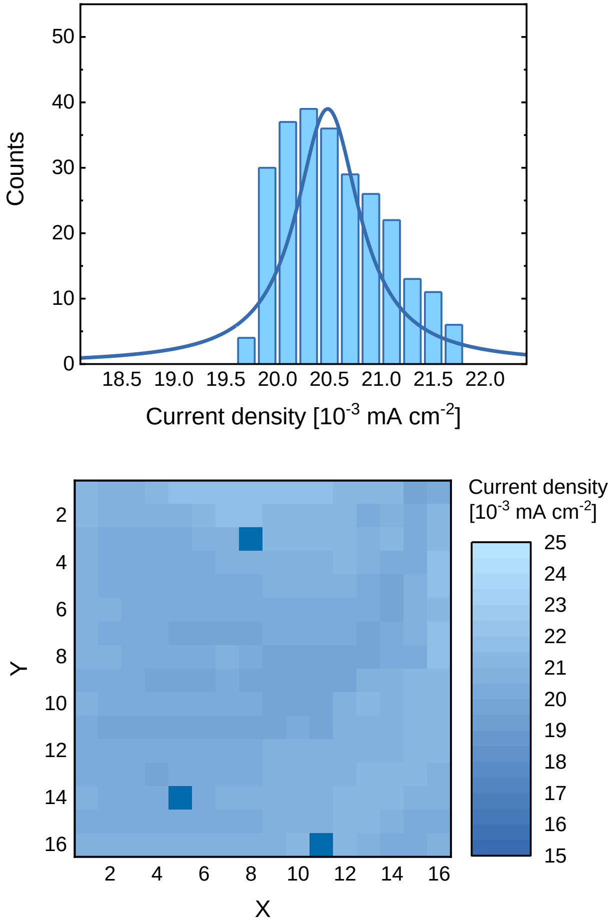
Pristine



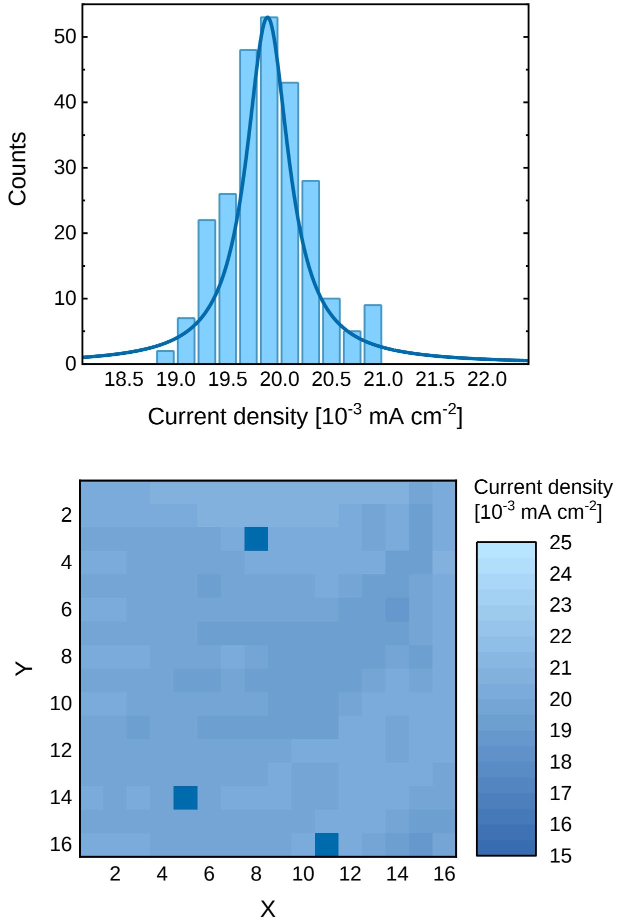
After PC lamination



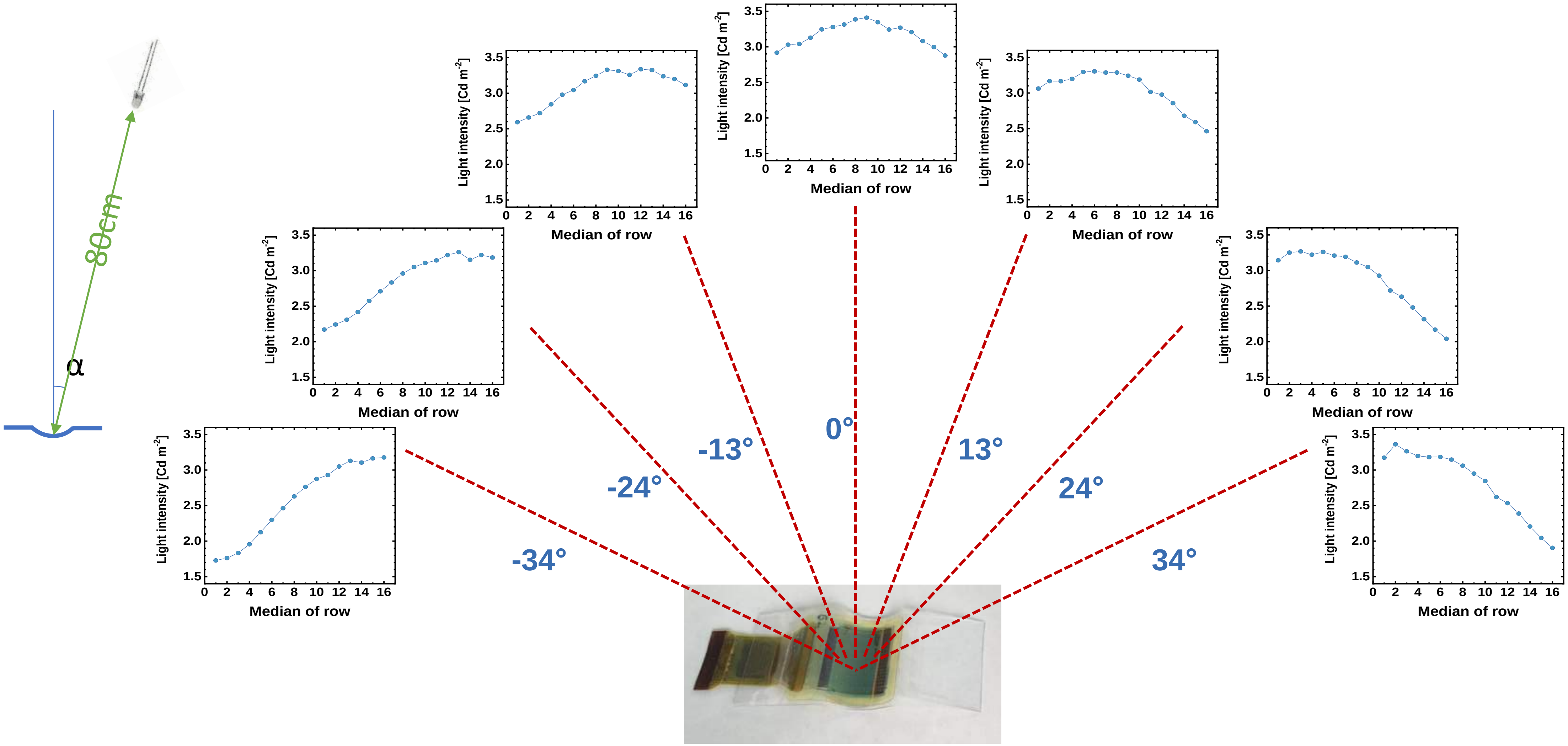
After laser delamination



After thermoform – no deform



Angle dependency : light intensity in Cd m^{-2}



Conclusions

- Technology developed for thermoforming and injection moulding of hybrid printed electronics
- Pilot line established with Flexlines partners
- Use case examples of light generation with sensors and imagining functionalities realised

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FLEXIBLE ELECTRONICS PROTOTYPING

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Thank you!

AGENTSCHAP INNOVEREN & ONDERNEMEN
Vlaanderen is ondernemen
Provincie Oost-Vlaanderen Voor ieder van ons
Provincie Noord-Brabant
provincie limburg gesubsidieerd door de Provincie Limburg
SMART HUB VLAAMS-BRABANT

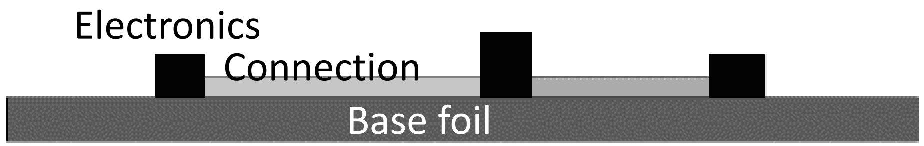
Injection over-molding of flexible electronics with engineering thermoplastics

Yibo Su, Ali Rezaei, Amandine Codou, Marc Huisman

TNO-Brightlands Materials Center

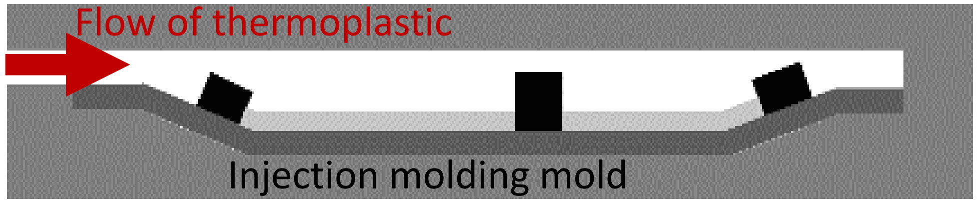
Introduction

Integrating flexible electronics into injection over-molded parts can be used to fabricate a lightweight structural component with integrated functionality (e.g. sensor, structural health monitoring, display)

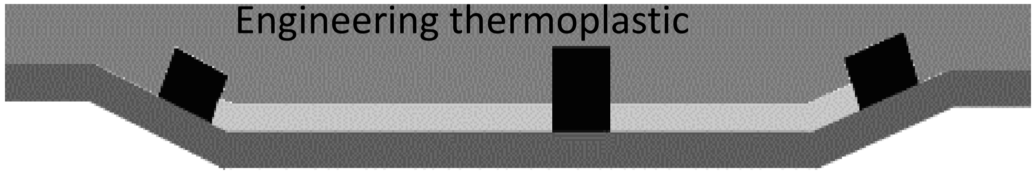


Step 1: Printing electronics on a flat foil to form the circuit

Step 2: Pre-forming the flexible foil circuit



Step 3: Injection over-molding with high stiffness and strength engineering thermoplastic



Final product

1. **Final product fulfills certain structural requirements**
2. **Utilizing adhesion between foil and thermoplastic to offer significant design freedom**

Video: The automated injection over-molding process suitable for multiple flexible electronics – engineering thermoplastics systems

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TNO innovation for life

Brightlands Materials Center

Holst Centre
Open Innovation by imec and TNO

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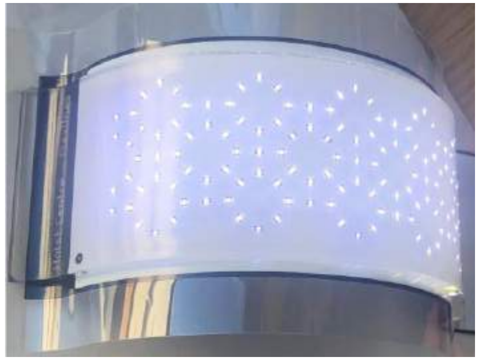
Goal and approach

Goal: A technical demonstrator with significant curvature (semi-circle) to demonstrate the design freedom provided by flexible electronics, which can be fabricated by different material systems:

- Engineering thermoplastics:
    - Polypropylene (PP), Polyamide (PA), Polycarbonate (PC)
    - With and without glass fiber reinforcement
- Two types of base foil for the flexible electronics:
    - Transparent: Polyethylene naphthalate (PEN) and Polycarbonate (PC) with silver printed connections
    - Non-transparent: Polyimide (PI) with copper cladded circuit



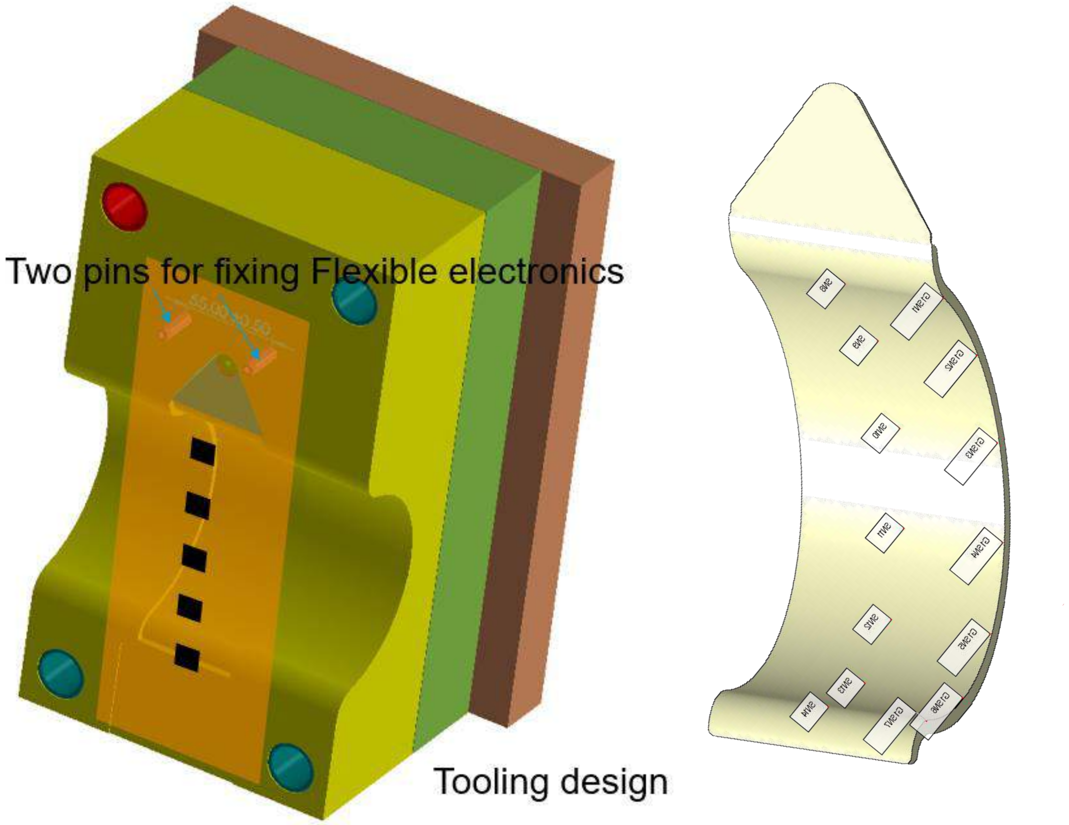
PEN foil + PC

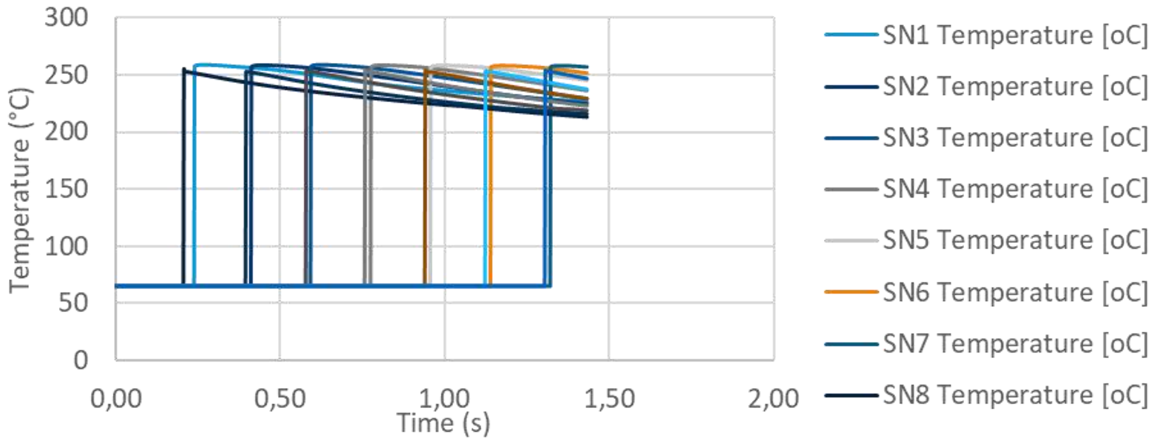
PI foil + PA

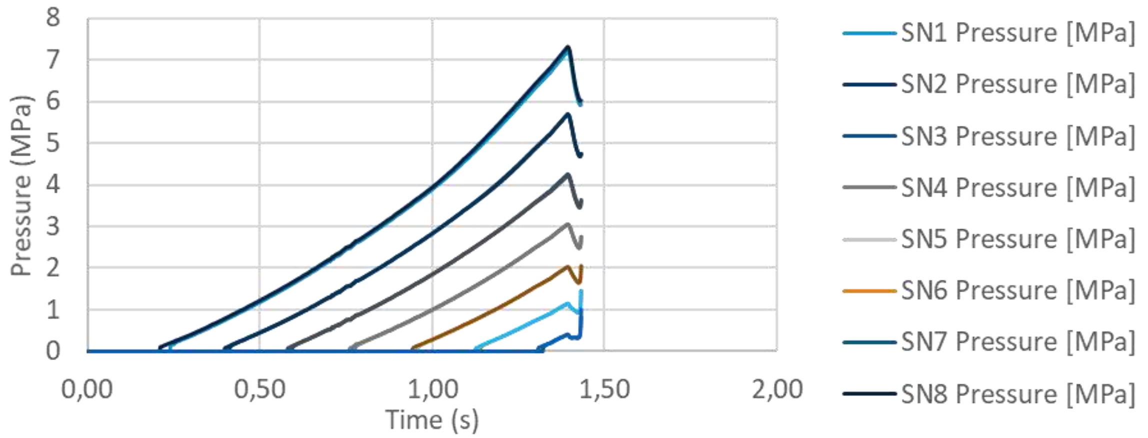
Challenges in designing and manufacturing of such a demonstrator:

1. High strength engineering thermoplastics usually requires high processing temperature and pressure:
    - **Approach: Understand the effect of these processing parameters on performance of electronics by advanced simulation technology.**
2. Engineering thermoplastic and base foil of flexible electronics are dissimilar materials.
    - **Approach: Optimize the adhesion between engineering thermoplastic and base foil with modified interface material and processing.**
3. The long-term performance of such injection over-molded flexible electronics under certain environmental condition is unknown.
    - **Approach: Evaluate the performance of the injection over-molded flexible electronics with accelerated environmental aging test, both in functionality and adhesion.**

Understanding temperature and stress of electronics in injection over-molding by applying advanced simulation technology





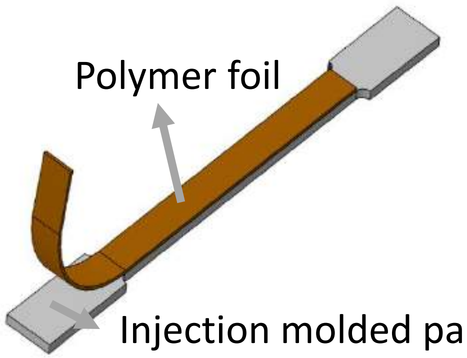


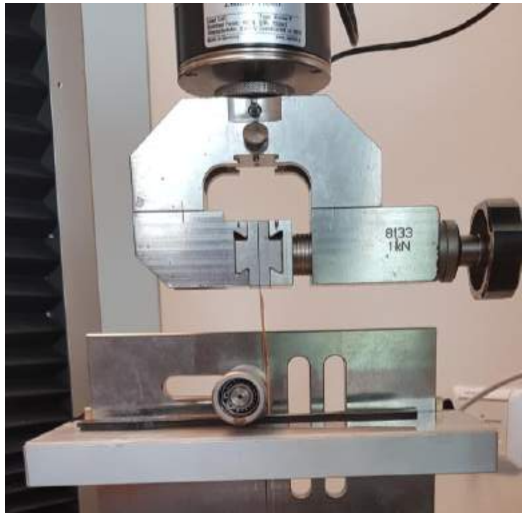
Example: Simulate temperature and stress on different locations within the mold cavity in the cavity filling process

Adhesion between foil and engineering thermoplastic

- Polycarbonate (PC) and Polyethylene naphthalate (PEN) based foil: Over-molded with PC thermoplastic offers good adhesion.
- Polyimide (PI) based foil: Traditionally, PI is used as release film in thermoplastic processing, thus proper coating required.

Method: adhesion evaluated by fracture energy based peel test

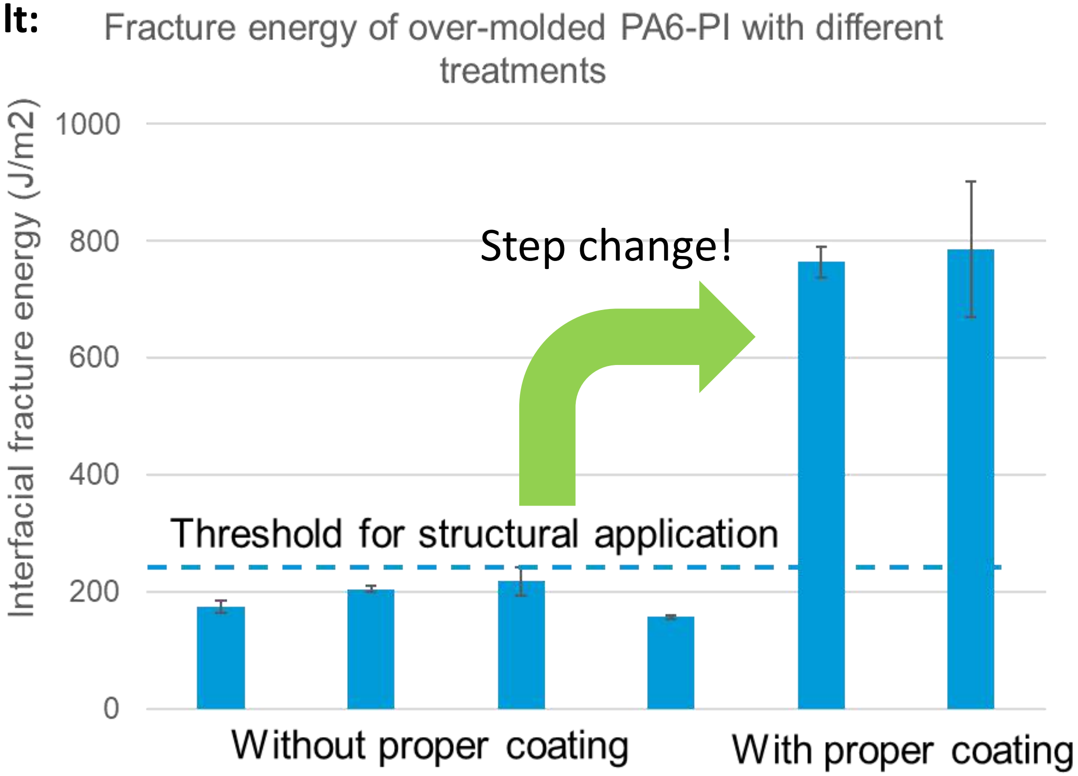




Interface separation force = Peel force - Foil plastic deformation force

(Mechanical property, thickness)

Result:



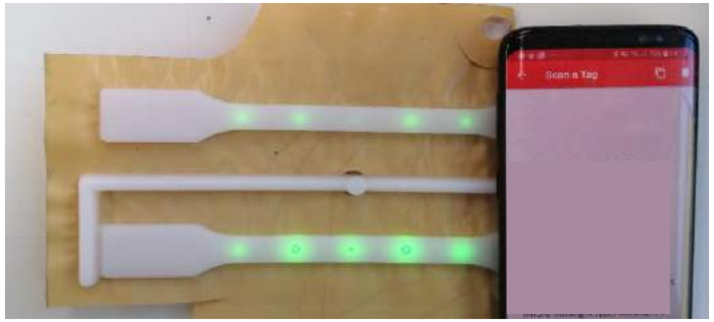
Long-term reliability test of over-molded electronics

Materials
PI foil - PA and PI foil – Glass fiber filled PA

2 Test steps

1. Aging samples under 80 °C/-40 °C fluctuations for 30 cycles according to ISO 16750-4
2. After checking cyclic aging, aging samples under 85°C/85% RH for 3000 h, which equals to approx. 100 years in 35°C/60% RH.

Study tools
Flexible PI foil with printed LEDs is over-molded with a "tensile test specimen" bar shape product, see figure



LEDs before aging

LEDs after aging

Conclusion:

- All of the LED samples printed on PI foils over-molded by both PA6 and GFPA6 **retain their function** after cyclic aging (Step 1) and 3000h static aging (Step 2).
- **Adhesion** between PI foil and GFPA6 is even **improved** after aging due to the high temperature further promote chemical bonding.

Summary and conclusion

- It is possible to well integrate flexible electronics into complex shaped engineering thermoplastic injection over-molded parts while retaining the functionality of electronics in long term use.

- The process of injection molding can be optimized through:
  - Suitable material treatment to achieve good adhesion.
  - Simulated electronic component temperature and stress to formulate an optimized circuit design.

Thank you!

Circuit Design Techniques with InGaZnO Thin-Film Transistors for Large Area Electronics

Mohit Dandekar, PhD Student,
MICAS-ESAT KU Leuven

Prof. Wim Dehaene (KUL)
Prof. Jan Genoe (imec/KUL)
Dr. Kris Myny (imec)

Technology overview

	Amorphous silicon	Organic	**Amorphous metal-oxide IGZO**	Low-temperature polycrystalline silicon	*Crystalline silicon*
Charge carrier mobility [cm²/Vs]	0.5	0.5-1.0	~10	~100	*~1000*
Bias stability	Poor	Poor	Reasonable	Good	*Good*
Max. process temperature	350°C	100°C	350°C	450+°C	*800+°C*
Carrier type	n-type	p-type n-type possible	n-type	CMOS	*CMOS*
Leakage current	Reasonable	Reasonable	Excellent	Poor	*Reasonable*
Critical dimension scalability	Excellent	Poor	Good	Poor	*Excellent*
Mask steps	4-5	4-5	4-5	6-9	*18-20*

Thin Film Technologies

Standard Silicon

IGZO-TFTs

Historical Development and Use →

- Current drive switch in display pixels
- Smaller, faster and less-leaky replacement for a-Si TFT in display technology*

Our Objective → Fully Integrated Circuits and Systems on Foil

Device → Ciruit Blocks → Functional Blocks → Integrated Systems

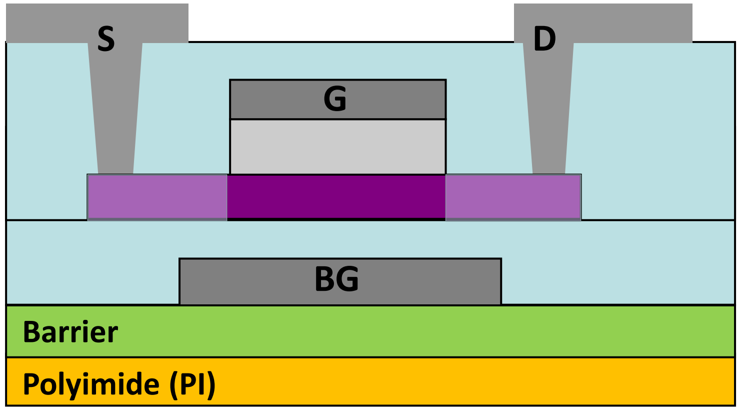
* Lorenz et. al., The 2016 Oxide Electronic Materials and Oxide Interfaces Roadmap. Journal of Physics D Applied Physics. 49. 433001. 10.1088/0022-3727/49/43/433001.

Circuit Design with IGZO-TFTs

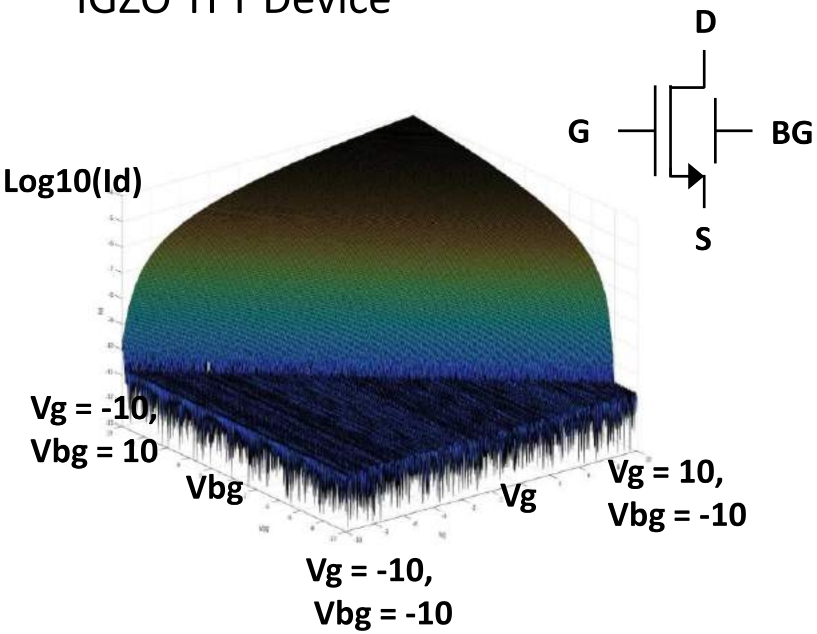
Flexlines Pilot Line → Dual Gate and Self Aligned Device

- MOS-FET type device
- Semiconductor thin film sandwiched between *two* gates
- Drain-Source symmetric operation
- Dual-Gate coupled channel control

Main Challenge → **Unipolar Device**



Schematic: Dual-Gate Self Aligned IGZO TFT Device



DC Drain Current Characteristics

Circuit Design with IGZO-TFTs

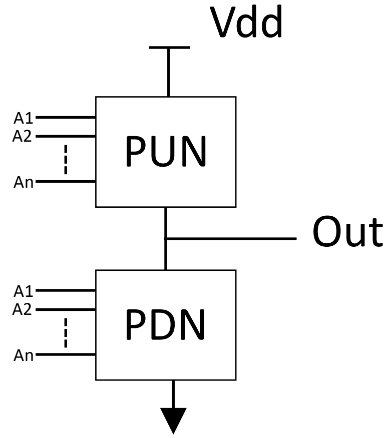
CMOS circuit design → matured research field, But….

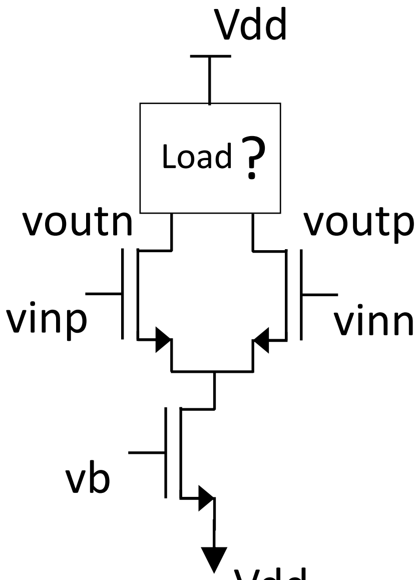
No Complementary (P-Type) Device in IGZO →

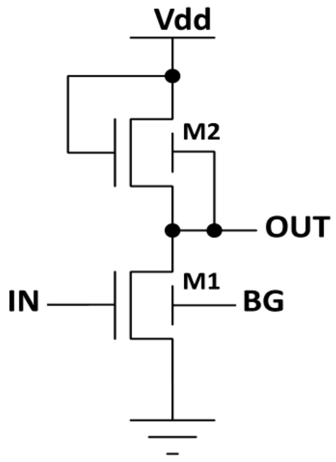
- How to make PUN
- How to make loads for gain stages

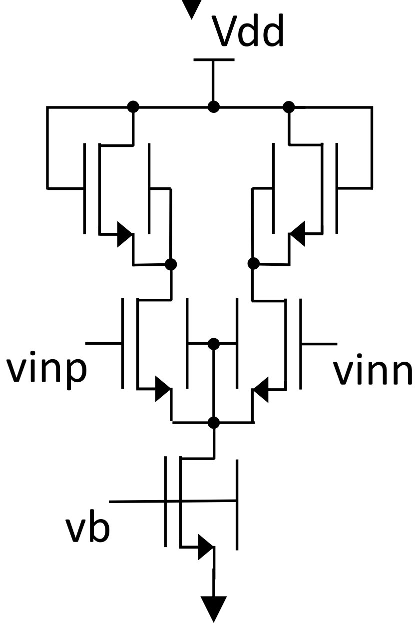
Solutions (Basic) → Use Ratioed Device

- Dual-Gate operation opens additional possibilities





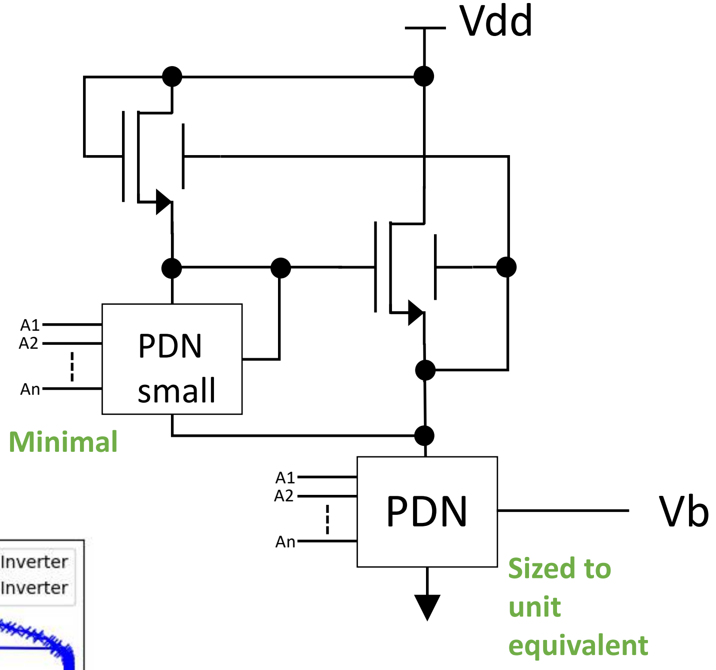


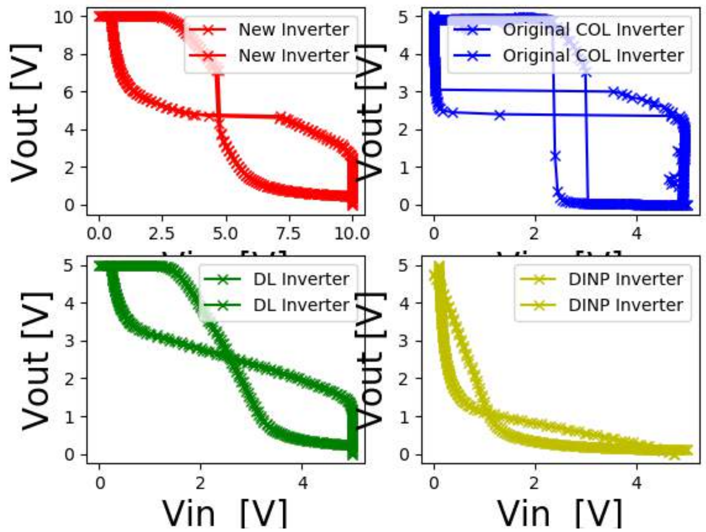


New Design Solutions -- Digital

Solutions (Basic+) → Enanced CrossOverLogic

- Based on input triggerred positive feedback
- Makes full use of dual gate operation
- Taped and measured April 2019



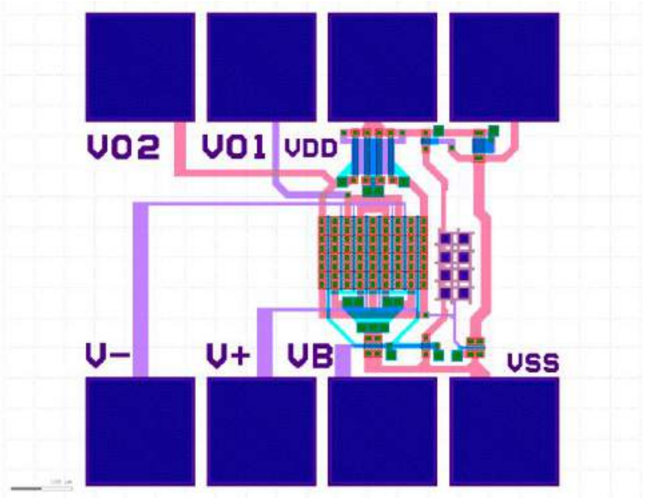


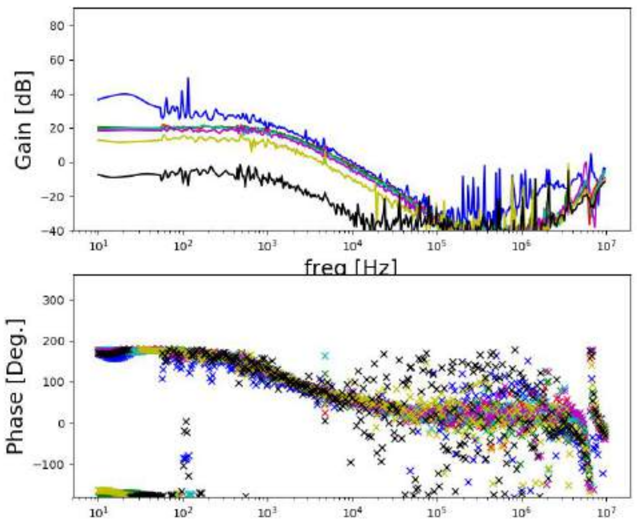
Original COL -- "F De Roose, J Genoe, W Dehaene, K Myny
IEEE Solid-State Circuits Letters 2 (7), 49-52"

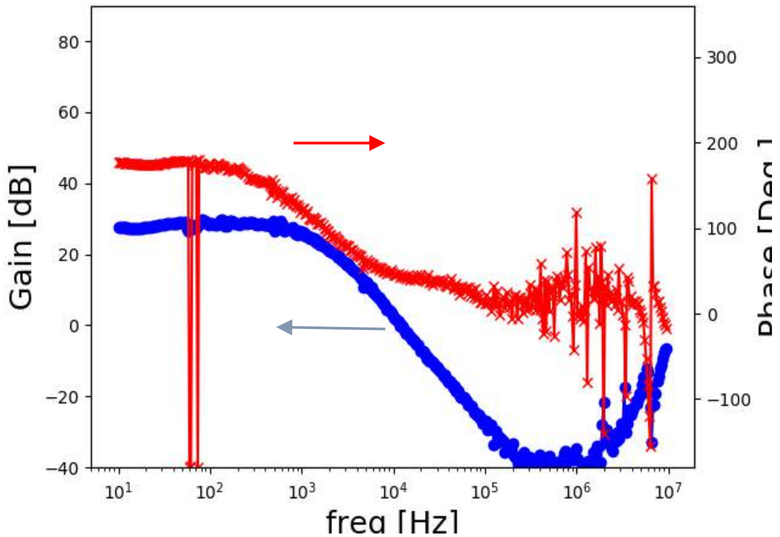
New Design Solutions -- Analog

Solutions (Basic+) → Two Stage Opamp

- Internal output feedback to increase impedance
- Makes full use of dual gate operation
- Taped and measured March 2020





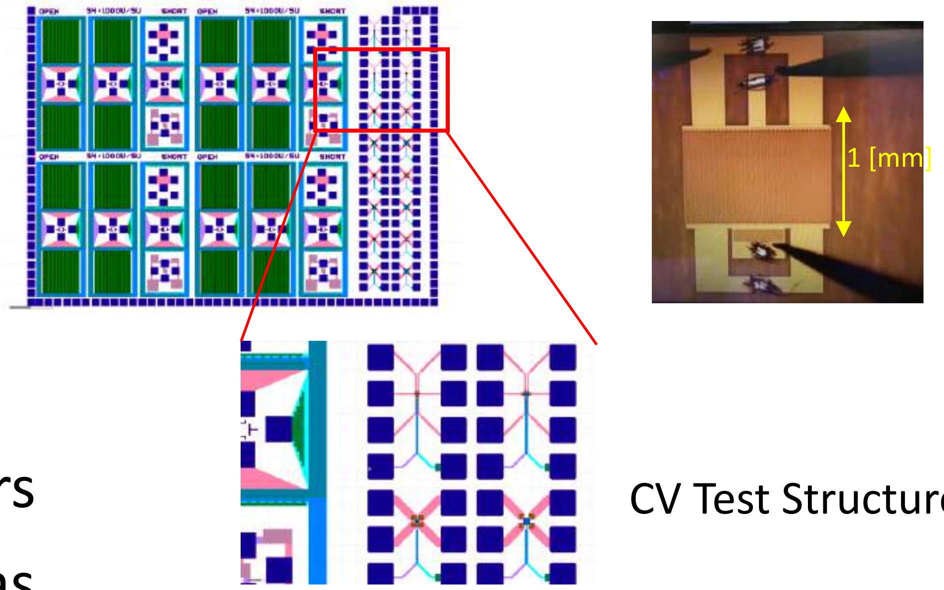


Measured
Open Loop Response

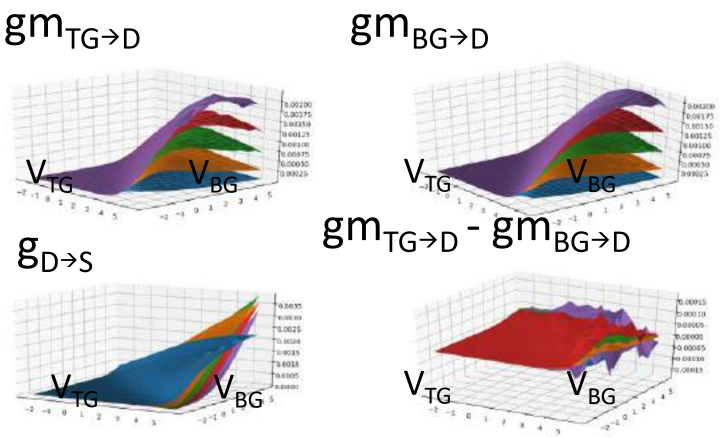
Device Modeling

Advanced Design → Need better device models

- Test structures taped to measure device parameters
- Measurement of small signal parameters under bias
- Hybrid Model – based on normalized operating point tables



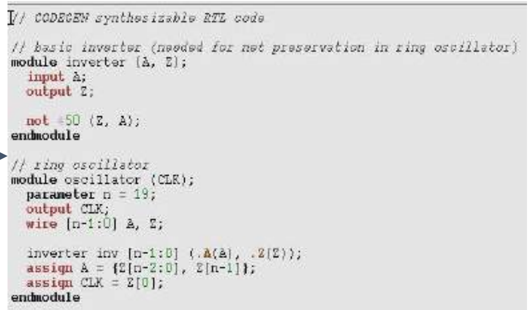
CV Test Structure



CV and small signal parameter measurement

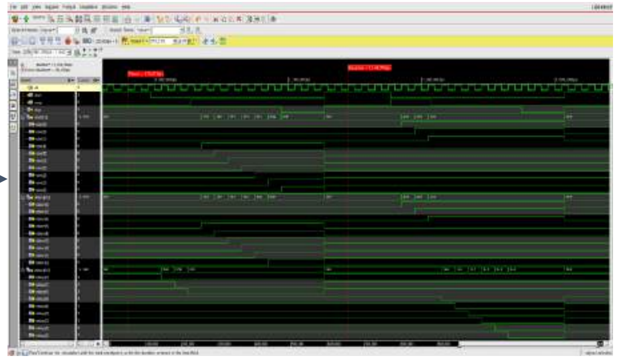
Semi-custom TFT design flow

HDL RTL coding

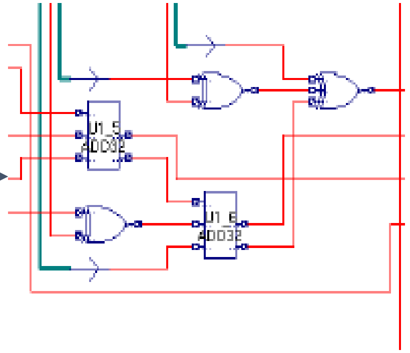


```
// CODEGEN synthesizable RTL code

// basic inverter (needed for net preservation in ring oscillator)
module inverter (A, Z);
  input A;
  output Z;

  not #50 (Z, A);
endmodule

// ring oscillator
module oscillator (CLK);
  parameter n = 19;
  output CLK;
  wire [n-1:0] A, Z;

  inverter inv [n-1:0] (.A(A), .Z(Z));
  assign A = {Z[n-2:0], Z[n-1]};
  assign CLK = Z[0];
endmodule
```

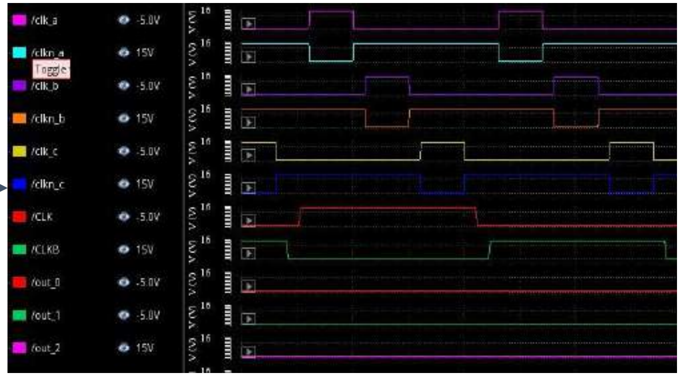
RTL simulations



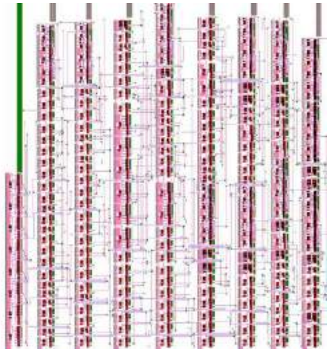
Logic synthesis



Gate level simulation



Place and route



Conclusions

- Main Challenge → Unipolar device circuit design

- Research Results
  - Use the unique dual-gate channel control to full benefit
  - Improve basic ratioed design with dual gate feedback
  - Prototype designs validated with tapeout and measurement
  - Test structures for measuring device parameters
    - Small signal parameters extracted via direct measurement
  - Development of custom design tool flow at imec Leuven

FLEXLINES
FLEXIBLE ELECTRONICS PROTOTYPING

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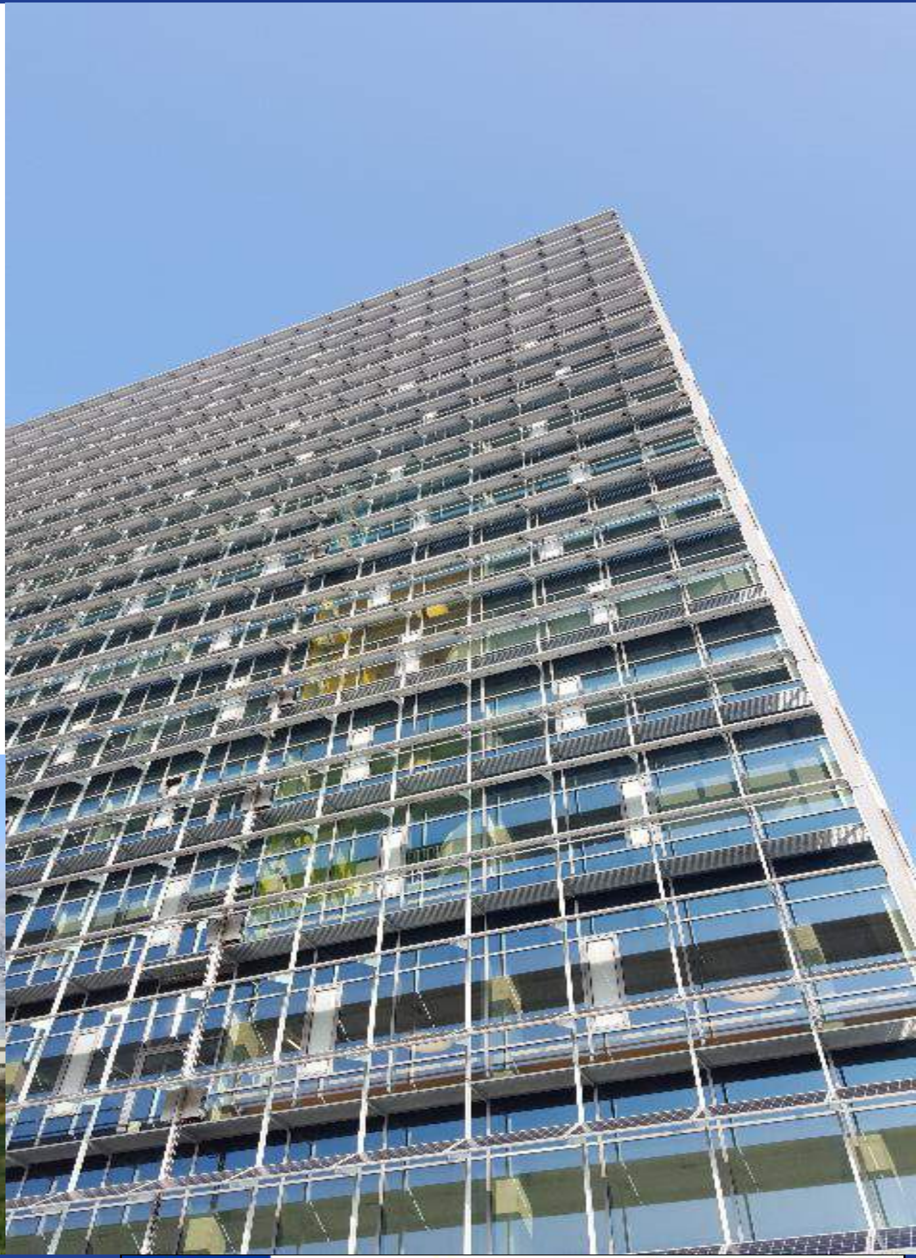
Electronics in the moulding process

Mona Bakr, Frederick Bossuyt and Jan Vanfleteren

CMST-Ghent university & Imec

CMST facts

- Research Group Center for Microsystems Technology
- Situated on the Technologiepark in Gent-Zwijnaarde
- Affiliated lab with imec and Ghent University
- Research group of ~ 50 people
- CMST is designing and developing microsystems such as implantable devices, smart contact lenses, optical sensors and devices for IoT



Introduction

What is injection moulding (IM)? –The technology to integrate electronics into plastics:

- Molten plastic is forced into a mould cavity under high pressure to make highly complicated parts at a near net shape with low part costs

- Process:
  Material preparation→ Feeding into the hopper→ injection →Mould holding and cooling → Ejecting

- Can be used in temperature monitoring in molds, wearables and automotive industries.

- Types:
  - Insert moulding
  - In-Mould labelling and In-mould decoration
  - Over-moulding

Introduction

Both technologies integrate and encapsulate printed electronics and standard electronic components within injection-moulded plastics.

Available technology -In mould

- A pre-printed label or decorated film is inserted into the open mould , and held in place with vacuum ports, where vacuum/thermoforming takes place
- Steps: Printing, surface mounting, thermoforming and injection moulding.
- Stacks of : Materials PC, functional inks and electronic components

CMST-OVM

- A single part is created using two or more different materials in combination. Typically the first material, sometimes referred to as the substrate, is partially or fully covered by subsequent material (over-mould material)
- Steps: Etching, surface mounting and injection moulding
- Based on polyimide flexible circuits technology

Aim of work

- Realize electronic circuits on PI-Cu foil in combination with over-moulding

  Challenges:
  1. Obtaining a good adhesion between foil and injection moulded plastics.
  2. Optimizing the injection moulding process so that the hybrid electronic circuits are not damaged.

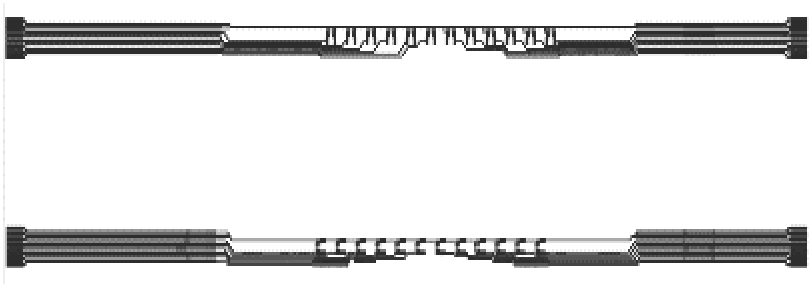
- Reliability tests and definition of functional requirements

  Challenges:
  To maintain the functionality of the electronic circuits (e.g. continuity of connections between components and printed foils)

Process flow

Over-moulded integrated foils

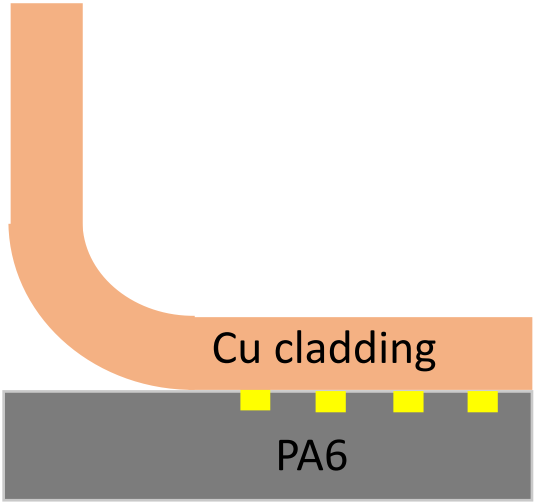
Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2



Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2

- Various techniques and PI foils types were used to optimize the adhesion.
- Three types of foils were patterned:
    1. Epoxy based adhesive foil
    2. Adhesive-less foil
    3. Acrylic based adhesive foil

- **The chosen foil must meet these conditions**:
    1. Adhesion between used foil and the injected plastic
    2. Electrical conductivity
    3. Ability to withstand over-moulding conditions (pressure and temperature)

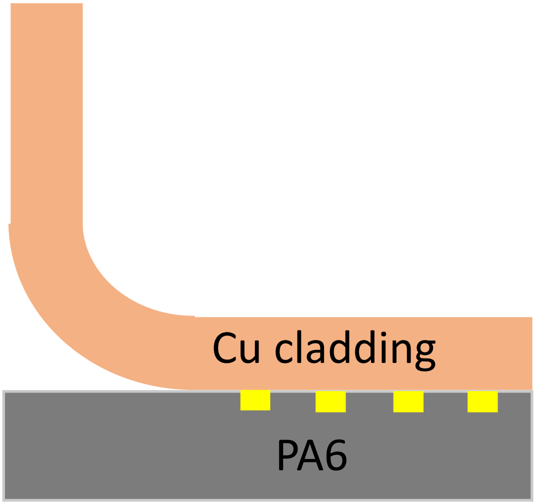


Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2

- Three types of foils were patterned:

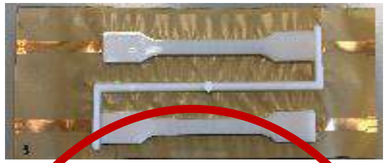


	Epoxy based adhesive foil	Adhesive-less foil	Acrylic based adhesive foil
Adhesion: Peel force(N) Interfacial fracture energy G_i (J/m^2)	Good 9.16 N 514 J/m^2	Worst 0.26 N 175 J/m^2	Best 15.2 N 703 J/m^2
Conductivity	Almost no data Foils were ripped after ovm	Showed data ,yet fluctuating high values	Values are more in the tolerance range
Withstand process	No	Yes	Yes



Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2

- Three types of foils were patterned:



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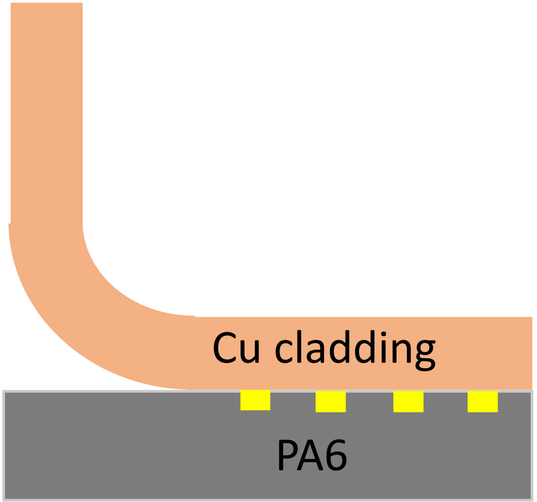
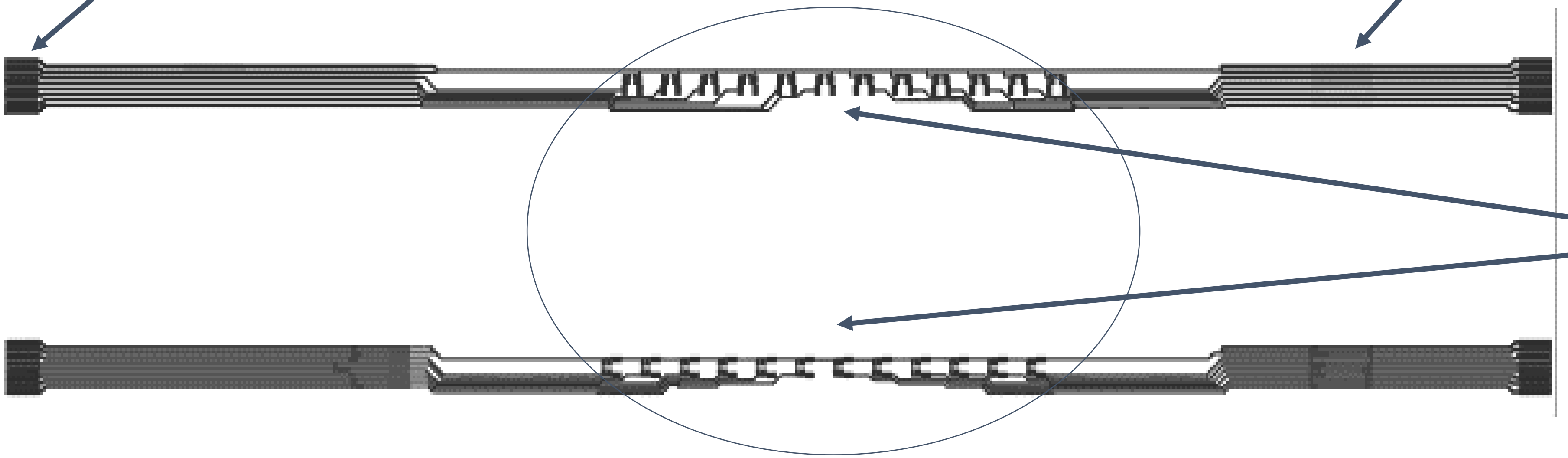


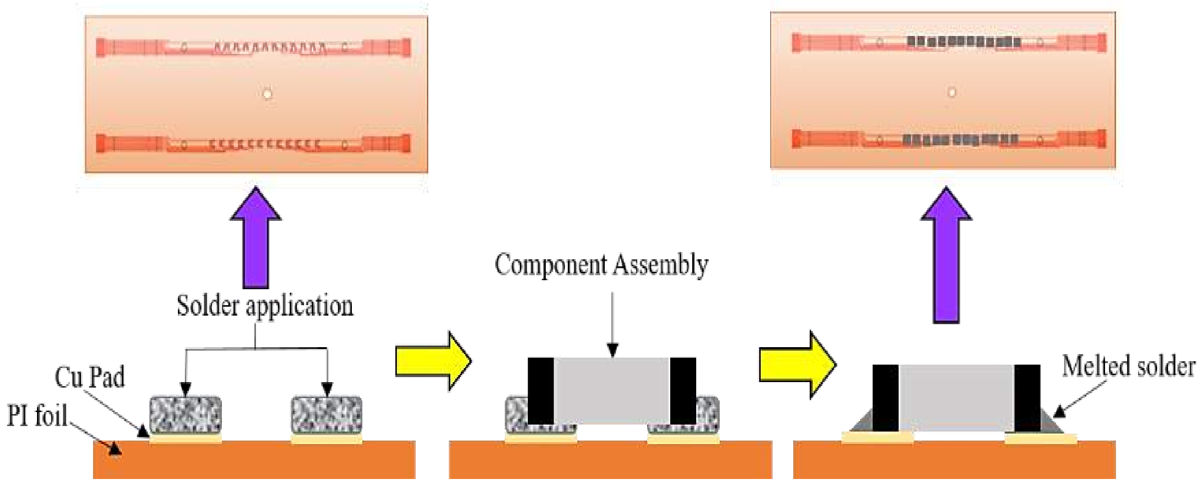
Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2

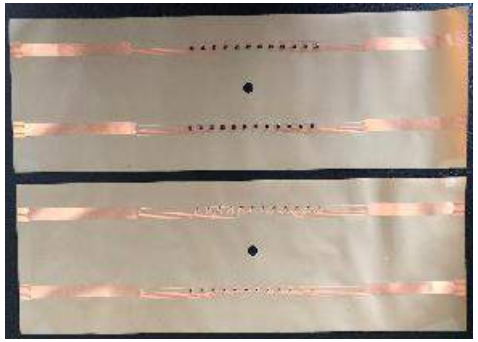
- This design is used as a preliminary design for testing, it:
  - can test different components sizes (1206,0402)
  - measures resistance easily

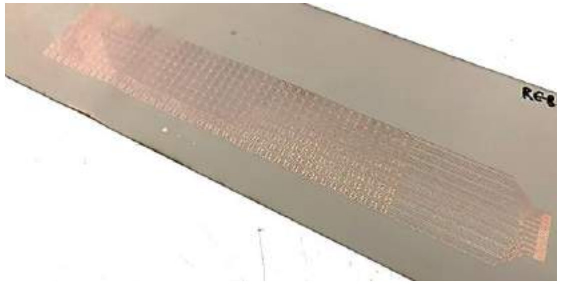


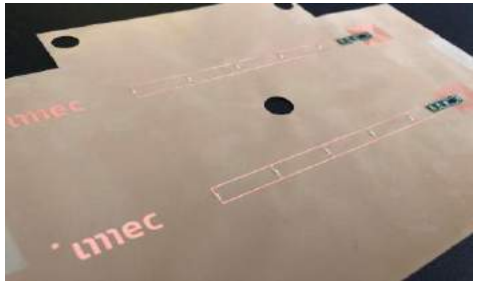
Adhesion check → Circuit design → **Foil preparation** → Over-moulding → Measurements → Demo-1 → Curved mold → Demo-2

- The process flow for flexible printed electronic includes patterning the copper structure on a flexible polyimide (PI) substrate via lithography and wet etching followed by an OSP treatment to protect the patterned copper from oxidation.
- Traditional lead free solder and under-fill materials were used.
- For technology check→ Resistor foils.
- For technology realization → NFC circuitry demo.
  → RGB matrix demo.



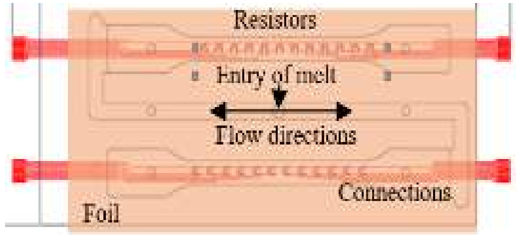


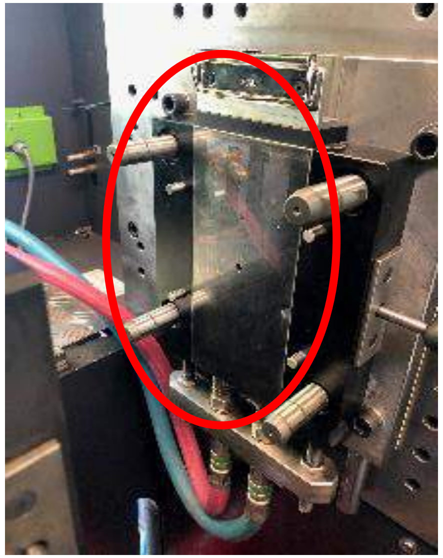


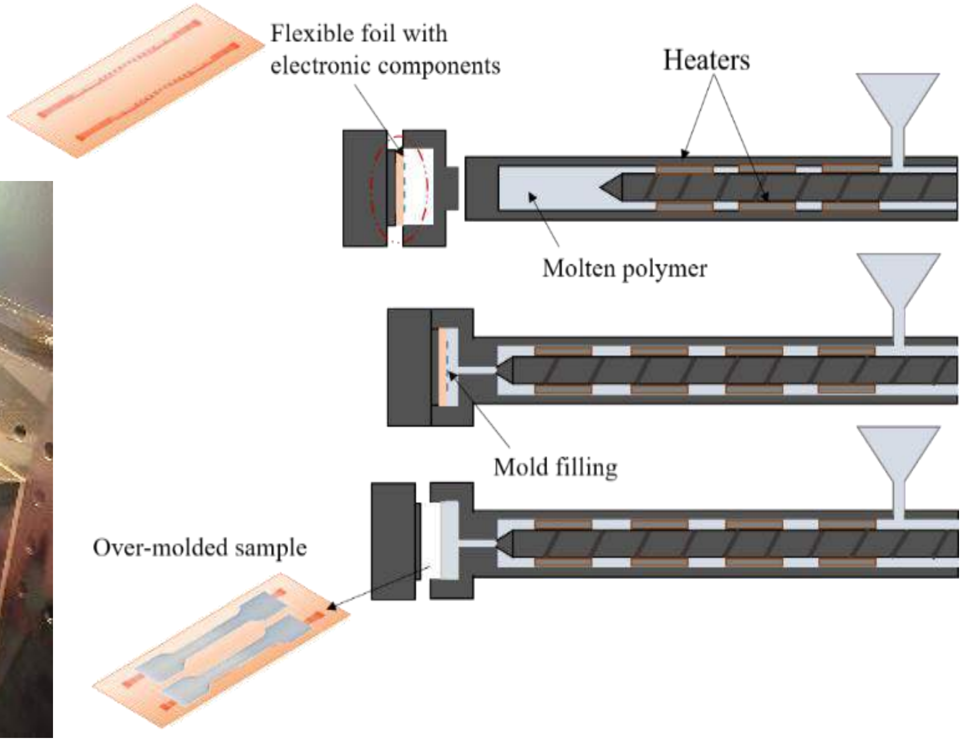


Adhesion check → Circuit design → Foil preparation → **Over-moulding** → Measurements → Demo-1 → Curved mold → Demo-2

- The integrated foil is clamped in the mould cavity then OVM process is performed where the polymer starts filing the mould and achieving the desired shape.
- OVM conditions: Melt Temperature 270°C
  Mold temperature 80 °C

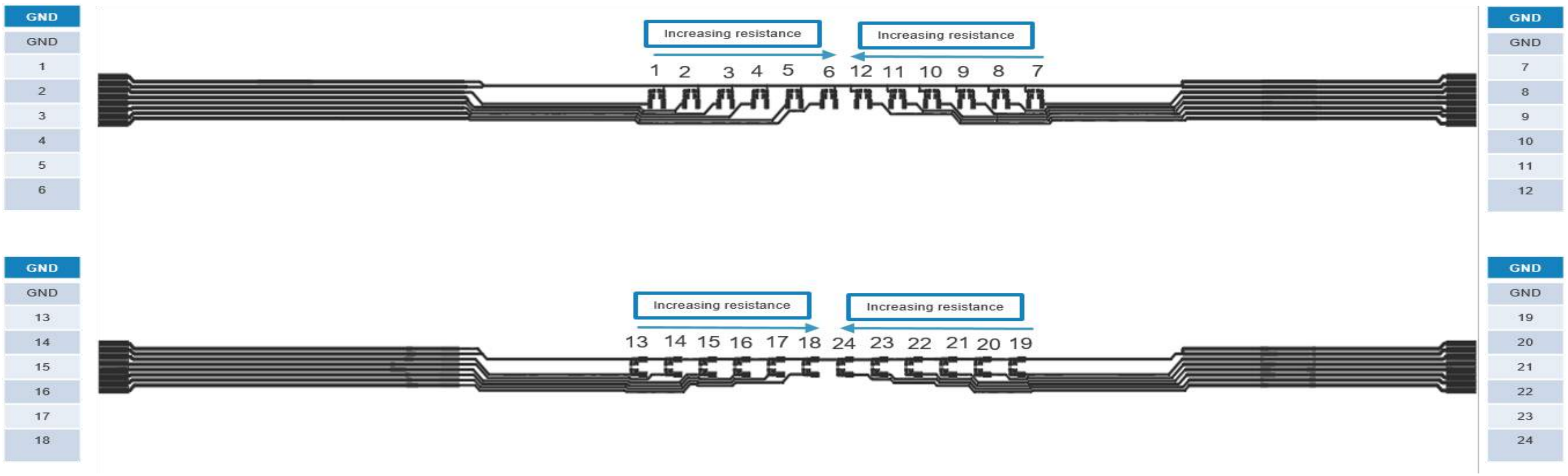






Adhesion check → Circuit design → Foil preparation → Over-moulding → **Measurements** → Demo-1 → Curved mold → Demo-2

- Using two-probe method.
- Connection check was done for 24 resistors before and after over-moulding.
- The overall resistance performance showed no difference between components size and resistors rotation.



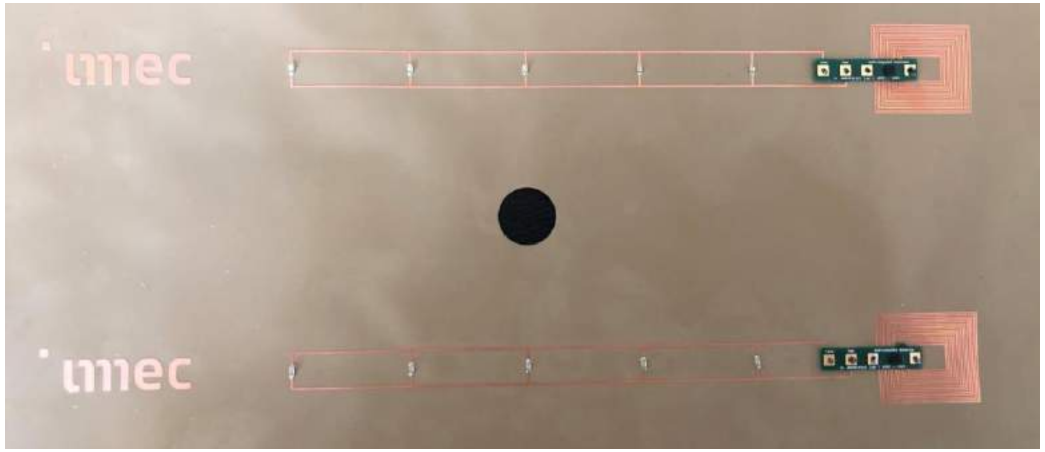
Adhesion check → Circuit design → Foil preparation → Over-moulding → **Measurements** → Demo-1 → Curved mold → Demo-2

- When the length increases the resistance increases in tolerance range of 0-Ω resistors.
- The data also shows that the mean value is 0.5 Ω.
- No difference was detected between the package sizes of the components.
- The rotation of the component in the flat mold didn’t influenced the measurements.
- After over-molulding, the resistance increases with increasing the temperature.

Foil	Resistor Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Resistance before OVM (ohms Ω)	0,4	0,5	0,5	0,5	0,5	0,6	0,4	0,4	0,4	0,4	0,5	0,5	0,4	0,5	0,5	0,6	0,6	0,6	0,4	0,4	0,4	0,5	0,5	0,6
1	**Resistance after OVM (ohms Ω)**	0,5	0,5	0,5	0,5	0,6	0,6	0,4	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,5	0,6	0,6	0,6	0,5	0,5	0,5	0,5	0,5	0,7
	Resistance before OVM (ohms Ω)	0,5	0,5	0,5	0,6	0,5	0,6	0,4	0,4	0,4	0,4	0,5	0,5	0,4	0,5	0,5	0,6	0,7	0,7	0,4	0,5	0,5	0,5	0,5	0,5
2	**Resistance after OVM (ohms Ω)**	0,5	0,5	0,5	0,5	0,6	0,6	0,4	0,4	0,4	0,5	0,5	0,5	0,5	0,5	0,5	0,6	0,7	0,8	0,4	0,5	0,5	0,5	0,5	0,5
	Resistance before OVM (ohms Ω)	0,4	0,5	0,6	0,6	0,6	0,7	0,4	0,4	0,5	0,5	0,5	0,6	0,5	0,5	0,5	0,5	0,5	0,6	0,4	0,4	0,4	0,4	0,4	0,5
3	**Resistance after OVM (ohms Ω)**	0,5	0,5	0,6	0,6	0,6	0,7	0,4	0,4	0,5	0,5	0,6	0,6	0,4	0,4	0,5	0,5	0,6	0,6	0,4	0,4	0,4	0,5	0,5	0,5
	Resistance before OVM (ohms Ω)	0,5	0,5	0,5	0,5	0,5	0,6	0,4	0,4	0,4	0,5	0,4	0,5	0,4	0,4	0,6	0,6	0,6	0,6	0,4	0,4	0,4	0,5	0,5	0,5
4	**Resistance after OVM (ohms Ω)**	0,5	0,5	0,6	0,6	0,7	0,8	0,4	0,4	0,4	0,5	0,5	0,5	0,5	0,6	0,7	0,6	0,6	0,6	0,4	0,4	0,4	0,5	0,5	0,5

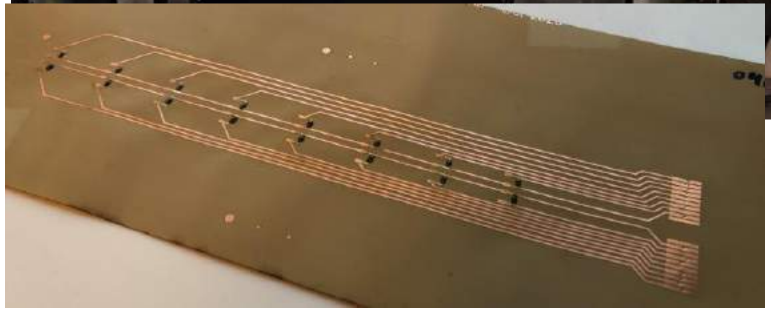
Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → **Demo-1** → Curved mold → Demo-2

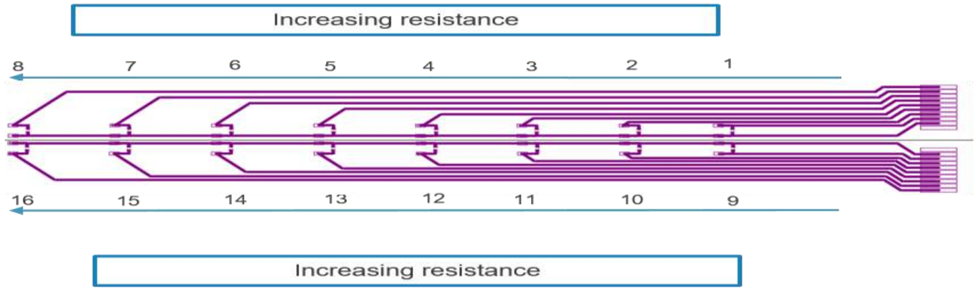
- The technology is shown by the realization of a demonstrator, in which LEDs are wirelessly powered using an NFC antenna and a chip.
- The NFC antenna is executed in the copper layer and the LEDs and NFC chip are soldered on the foil.
- The antenna and NFC chip can harvest the energy from (e.g. a smartphone) in order to power the LEDs.
- After over-moulding → All LEDs are functional.

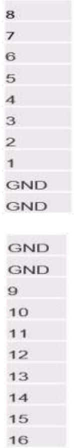


Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → **Curved mold** → Demo-2

- To check the influence of a curvature mould on the components.
- The design is as follows:
  - 20 components in 90° orientation
  - Resistors and LEDs in (1206,0402) packages can be used



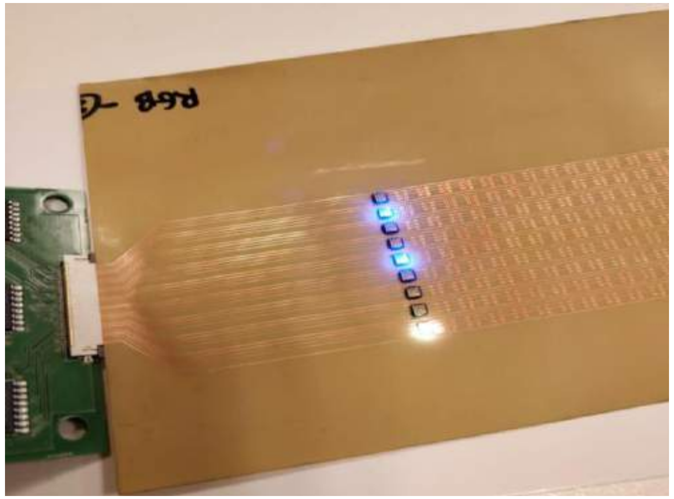


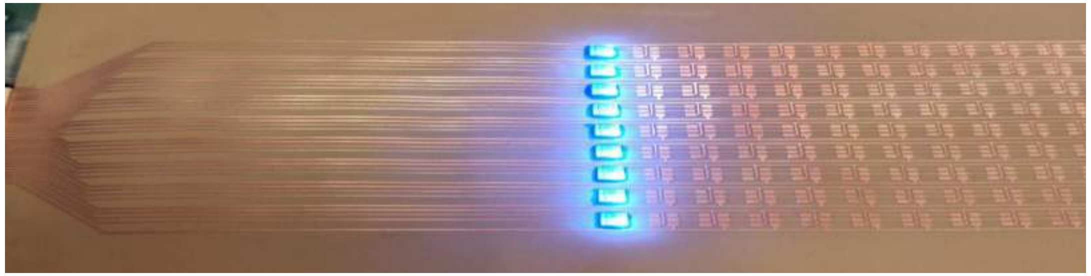


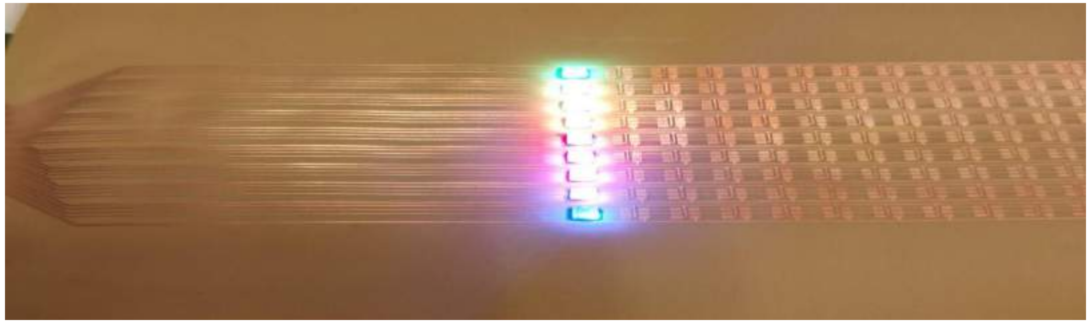
	#	Component size	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1206	1	1206 -270°C	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,5
	2	1206 -270°C	0,2	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,5
	3	1206 -270°C	0,2	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,5
0402	1	0402-270°C	0,2	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,5
	2	0402-270°C	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,4	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,5
	3	0402-270°C	0,2	0,3	0,3	0,3	0,4	0,4	0,5	0,4	0,2	0,3	0,3	0,4	0,4	0,4	0,4	0,5

Adhesion check → Circuit design → Foil preparation → Over-moulding → Measurements → Demo-1 → Curved mold → **Demo-2**

- Our design is as follows:
  - Matrix of RGB LEDs connected with a board to show logos as a display
  - As a preliminary testing a column of LEDs is assembled to check the connection to the board and to check the over-moulding.
  - Final demo will be finished in the coming weeks.







Conclusions

- Preliminary functional test circuits proved that their electronic interconnections can withstand both thermal and mechanical stresses provided from the over-molding process.
- Adhesion was achieved between PI/Cu foil and PA6 as an injected plastic.
- Reliability of these test structures showed good performance on long term application.

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Thank you!

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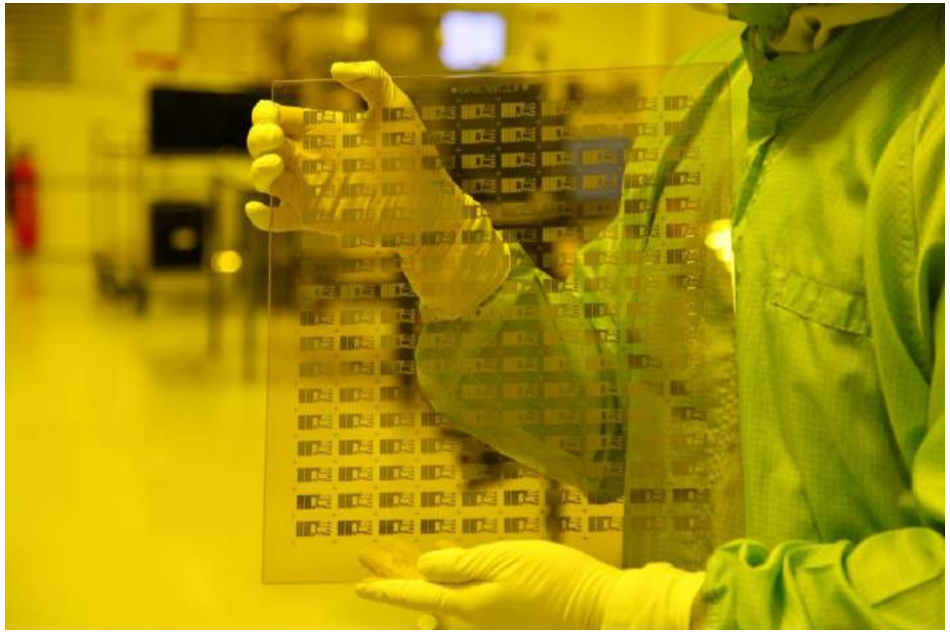
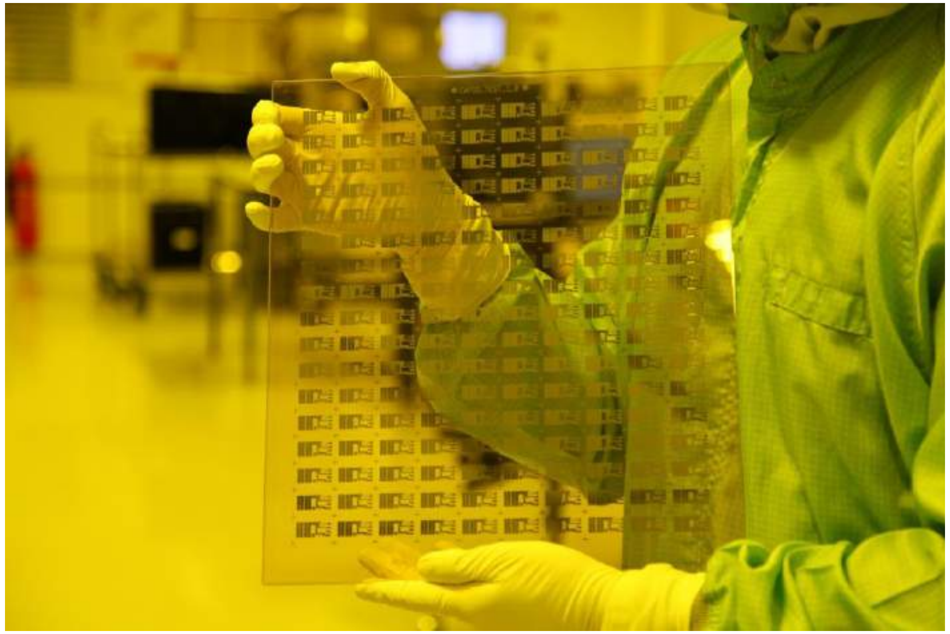


Concluding remarks

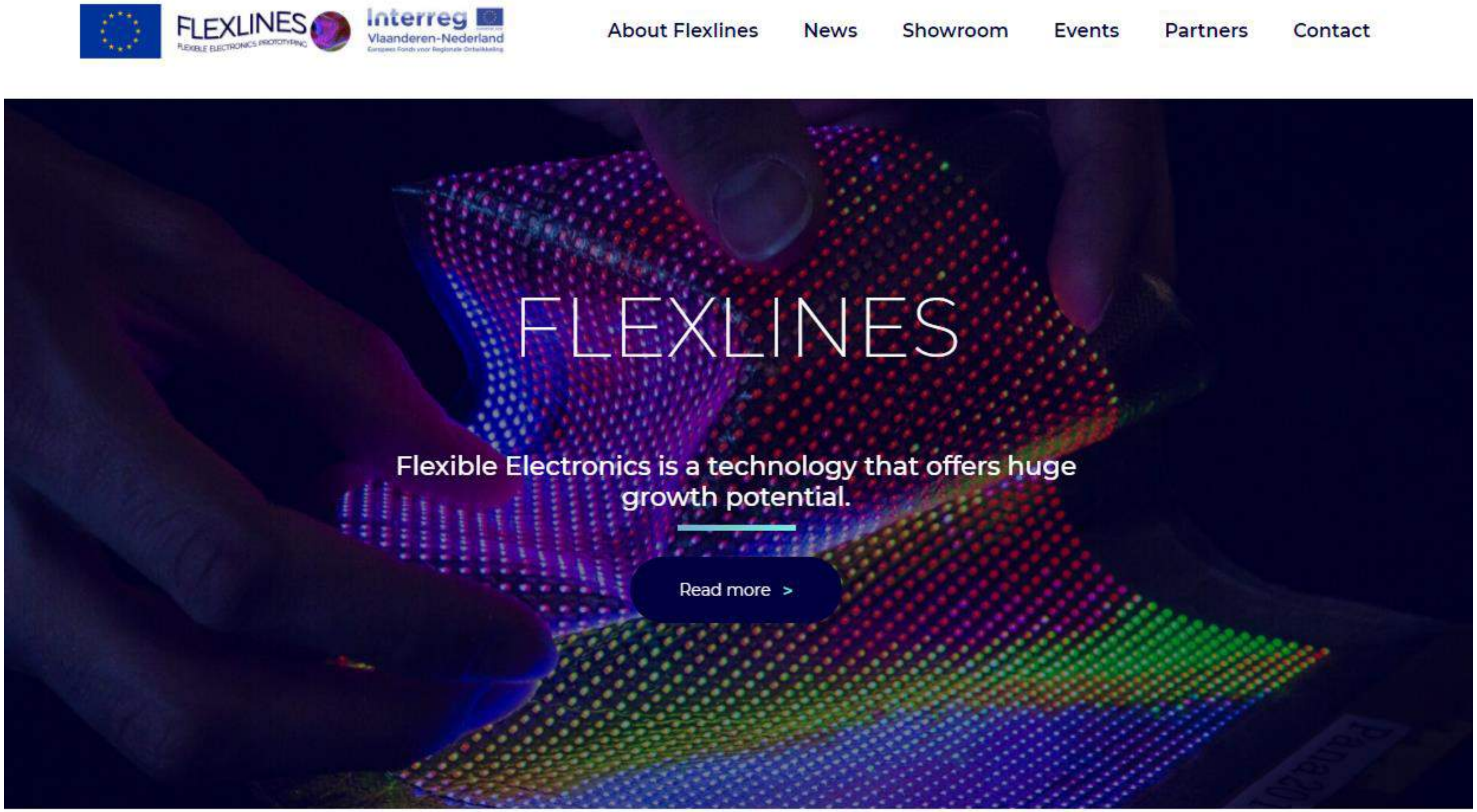
Conclusions



- FLEXLINES has proven to be a fabrication route, where academia and companies can realize their ideas in flexible and cheap electronics-applications.

- For more information:
  - FLEXLINES pilot line : Auke.Kronemeijer@tno.nl
  - One-Stop-Shop: Romano.Hoofman@imec.be

Flexlines website



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INTEGRATION OF ELECTRODE ARRAYS IN MICROTITER PLATES
Biochemical experiments are generally performed in standardized microtiter wellplates according to ANSI/SBS standards. Therefore, integrated electronic readout of microbiological systems need to be rendered compatible with these standards. Flexlines realized a number of prototype demonstrators have been realised for the introduction of Metal Electrode Arrays (MEAs) and high density Active-Matrix Electrode Arrays into (3D printed) COC microtiter plates. The added value of large-area mesh electronics – high density electrode array membranes with open structures in between the electrode pads – has been demonstrated by realisation of suspended electrode arrays in multiwells, enabling fully 3D growth of tissue around the electrode arrays.
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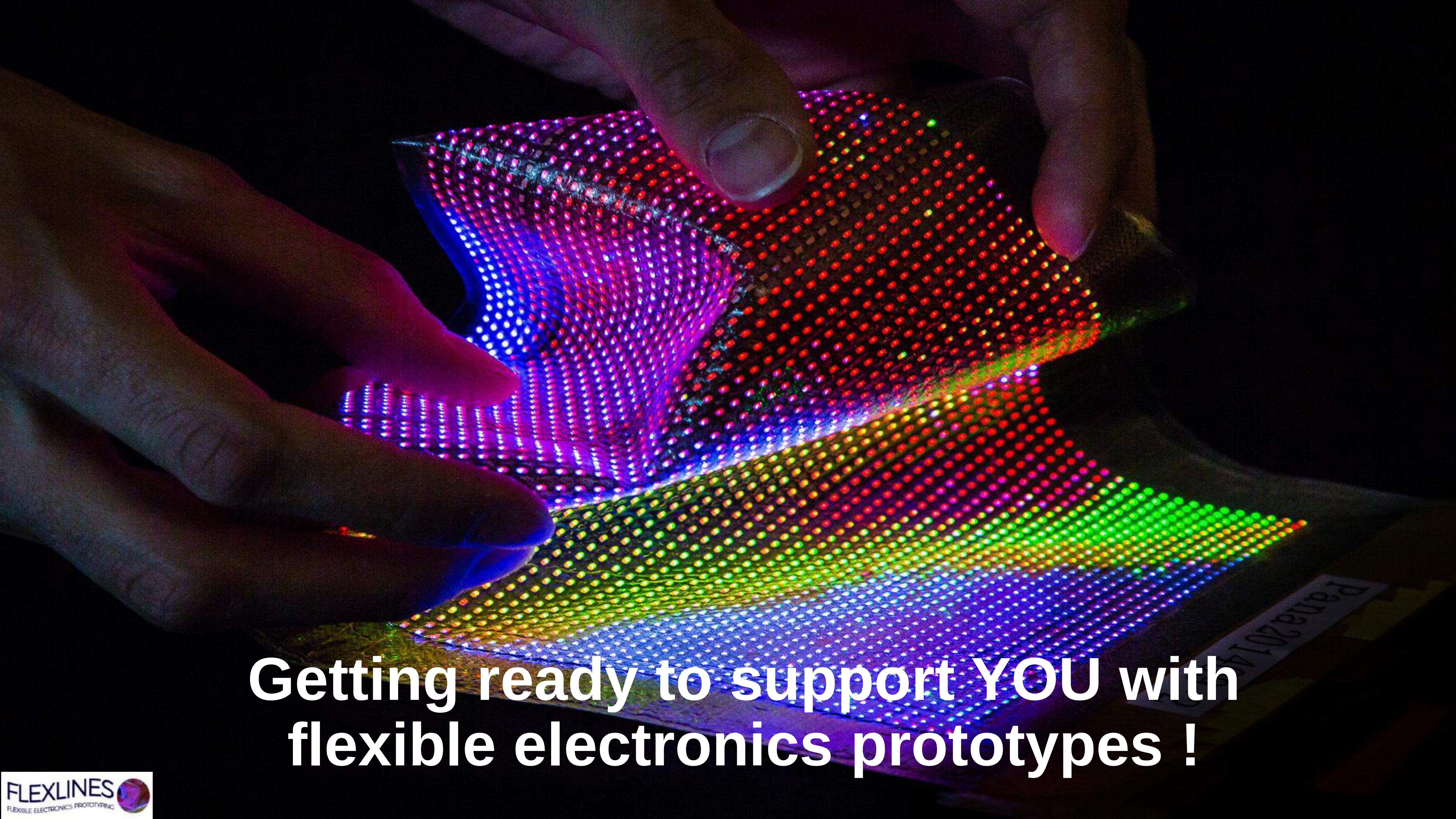
FLEXLINES ENABLING FLEXIBLE ELECTRONICS PROTOTYPES
Flexlines has developed and coordinated the individual links in the Flexible Electronics value chain: processes and infrastructure for design and production. The consortium of partners set up a state-of-the-art and stable pilot line and a 'one-stop-shop' for the realisation of Flexible Electronics prototypes.
Prototypes that meet the needs of the local industry in the border region have been realised for validation of the technology. The main prototypes are showcased in this flyer.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