Multiple-Output Switched-Capacitor DC-DC Combination Converters for IoT Applications

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***Abstract*— This paper presents and describes switched-capacitor DC-DC combination converters with a single input and multiple outputs, with step-down and step-up voltage ratios. The combination converters provide two or three different DC outputs (depending on the combination), with different conversion ratios. The main advantage of the proposed converters is the low number of components used in the combination (two-output configurations require two link capacitors, and three-output configurations require three link capacitors) and two complementary phase clocks, which may reduce size and manufacturing costs for many applications. The DC-DC combination converters are designed to be fully integrated, and were implemented in a 65nm CMOS technology. The analysis of the proposed configurations for different performance modes and load conditions is presented, and simulation results show that these combination converter topologies are suitable for multiple-output switched-capacitor DC-DC converters with multiple conversion ratios.**

Keywords*— *Switched-capacitor, DC-DC converters, Single-input multiple-output, IoT.

I. Introduction

DC-DC switching-mode converters, without inductors and transformers, are a good option for several power supply applications, especially for small format electronics systems and integrated circuits (IC). Converters that only use capacitors and switches are generally called switched-capacitor (SC) converters. They operate using a capacitive energy transfer by adjusting the charging and discharging periods of the SC. Applications such as IoT (Internet-of-Things), implantable medical devices and/or wireless sensor networks are good examples where reduced sizes in power supplies are a key feature [1]. In general, these applications are powered by small batteries, and require power-supplies with low electromagnetic interference (EMI), small size and weight, high power density integration and low losses. In this way, SC DC-DC converters fit like a glove in the IoT domain, because they allow monolithic substrate integration due to the reduction of silicon surface required and size, and contribute towards reduced electromagnetic effects and power losses.

Traditionally, SC DC-DC converters have been used to provide simple, unregulated power conversion at lower power levels [2][3][4][5]. Recent developments in capacitor and semiconductor technology have made switched-capacitor DC-DC converters more useful in higher power applications [6][7][8][9][10]. Furthermore, the development of new control strategies has also added voltage regulation capabilities to SC converters, as it can be seen in DC-DC converters for LED driver applications [11][12]. These developments have contributed to the increasing popularity of SC converters, both in integrated form and in discrete circuits.

Recent publications show that on-chip MOS capacitors can be used in SC DC-DC converters to achieve a fully integrated converter DC-DC with low series resistance and high capacitance density, and they do not require any additional fabrication steps [13]. As an example, the work in [1] presents a high efficiency all-CMOS switched-capacitor DC-DC converter (SC DC-DC) with frequency, switch size and interleaving scaling, to achieve high efficiency for wireless sensors and IoT applications. In [14], authors propose a highly efficient SC DC-DC converter, which is implemented in a 65nm low power CMOS process to enable system on chip (SoC) integration. The step-down converter operates with a constant input voltage of 1.83V and produces an output voltage of 1.2V.

IC implementations of DC-DC converters use normally step-down configurations, i.e., configurations where the output is smaller than the input voltage. Moreover, many solutions appear for single output converters, but to reduce power consumption in today's IoT chips, aggressive power reduction techniques are being increasingly used and require multi-domain power supply outputs [15]. As explained in [16], to achieve ultra-low energy consumption levels in these new IoT chips, Adaptive Voltage and Frequency Scaling (AVS) techniques and Dynamic Voltage and Frequency Scaling (DVFS) techniques should be used, to work at different power supply voltage (V_{DD}) and clock frequency levels.

The generation of different DC outputs voltage levels, from one DC input with SC converters can contribute significantly in countless applications in this new Internet-of-Everything (IoE) era, due to the increased on-chip power management and miniaturization requirements in today's IC. These applications require multiple outputs from the same power supply with step-

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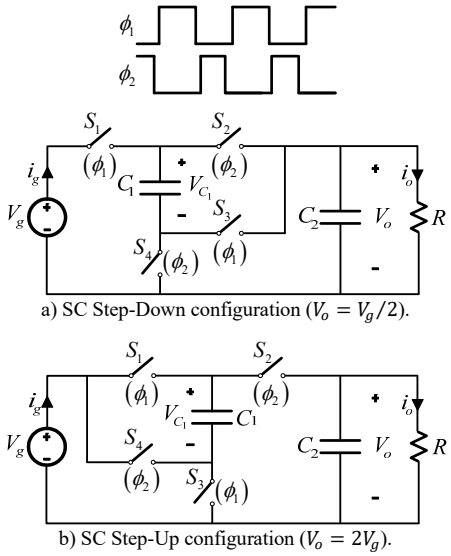
down and step-up conversion ratio. Single-input multiple-output SC (SIMO SC), are particularly interesting for interfacing with different sources and energy storage systems, as well as different loads' requirements.

This work presents a methodology for SIMO SC based on single-input switched-capacitor converters. The methodology has allowed to derive configurations for two different DC outputs, and configurations for three different DC outputs, using both step-down and step-up conversion ratios. The main advantage of the proposed converters is the low number of components used, which reduces the overall size and manufacturing costs.

The reminder of the paper is organized as follows: in Section II, the new topologies are presented and analyzed, and the main voltage relations are detailed; in Section III, the simulation models are described and the converters behavior is verified for several loads and performance modes; in Section IV, some conclusions are given and future work perspectives are presented.

II. Proposed Topologies

Fig. 1 shows two basics switched-capacitor DC-DC converters, with step-down and step-up conversion ratio. S_1-S_3 are a pair of synchronized switches (controlled by ϕ_1), and S_2-S_4 are complementary to the prior ones and controlled by ϕ_2. The phase signals ϕ_1 and ϕ_2 are two complementary and non-overlapping clock pulses, to avoid shoot-through states. The switches alternately connect the capacitor C_1 with the input source (V_g), or with the output capacitor C_2; C_1 acts as a path to transfer energy from the input to the output. Both SC converters, step-down and step-up topologies, used one link capacitor and require four switches. The output capacitors guarantee a low ripple at the output and store the energy transferred from the link capacitor.



a) SC Step-Down configuration ($V_o = V_g/2$).

b) SC Step-Up configuration ($V_o = 2V_g$).

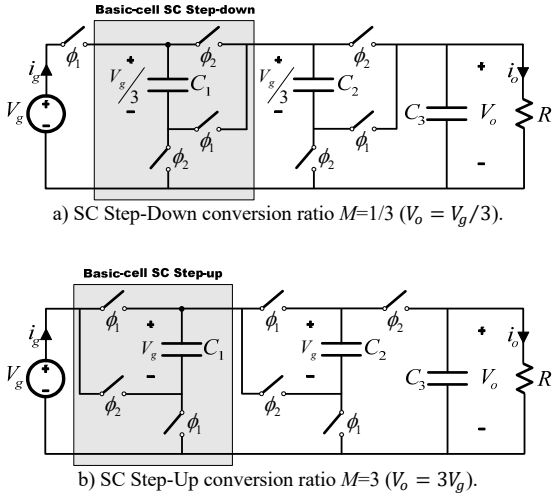
Fig. 1. Basic switched-capacitor converters.

Equation (1) presents the step-down and step-up voltage conversion ratios (M) for the steady-state regime.

$$M = \frac{V_o}{V_g} = \frac{1}{2} \quad \text{for basic-cell SC step-down}$$
$$M = \frac{V_o}{V_g} = 2 \quad \text{for basic-cell SC step-up} \tag{1}$$

The values in (1) are obtained assuming SC converters without losses (equivalent series resistance of capacitors and switch resistances negligible), and ignoring the dependencies of the capacitance values, switching frequency and clock duty cycle.

A characteristic of switched-capacitor DC-DC converters is that the conversion ratio M, for step-up or step-down, is a rational number p/q where p and q are positive integers smaller than the n^{th} Fibonacci number [5], where n is the number of capacitors used and $3n$-2 the number of switches required to realize the converter. For example, with three capacitors (n=3), two link capacitors and seven switches, a conversion ratio M=3 (step-up) or M=1/3 (step-down) can be obtained, as shown Fig. 2. Therefore, as done in other non-SC DC-DC converters [17][18], from basic-cells connected in cascade, it is possible to obtain SC converters with different conversion ratios. From the analysis of the two switched-capacitor DC-DC converters shown in Fig. 2, it can be observed that both converters have common parts, which can be combined to obtain converters with two outputs. An example is shown in Fig 3, where sharing a link capacitor (Fig. 3.b), or simply sharing the input source (Fig. 3.a), to obtain two different DC outputs, with step-up and step down conversion ratios, with outputs define by equations (2) and (3). In this way, it is possible to generate two-output configurations by combining known SC topologies, reducing space and implementation costs.



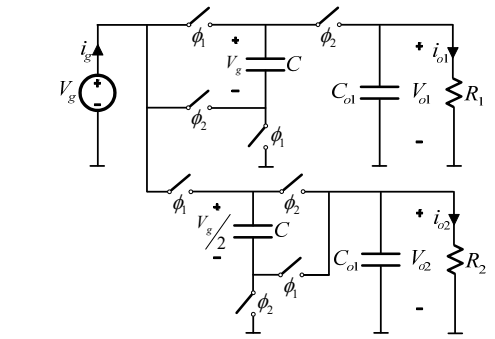
a) SC Step-Down conversion ratio M=1/3 ($V_o = V_g/3$).

b) SC Step-Up conversion ratio M=3 ($V_o = 3V_g$).

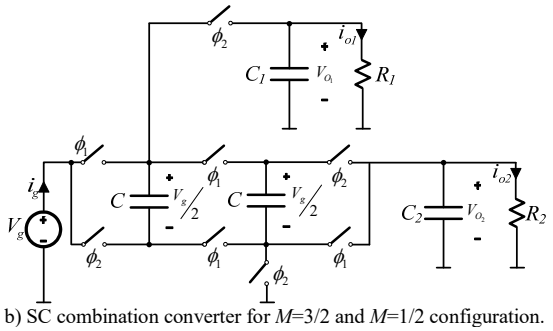
Fig. 2. Switched-capacitor converters with two basic-cells.

$$\text{For Fig. 3(a):} \quad V_{o_1} = 2V_g \text{ and } V_{o_2} = \frac{V_g}{2} \tag{2}$$

$$\text{For Fig. 3(b):} \quad V_{o_1} = \frac{3V_g}{2} \text{ and } V_{o_2} = \frac{V_g}{2} \tag{3}$$

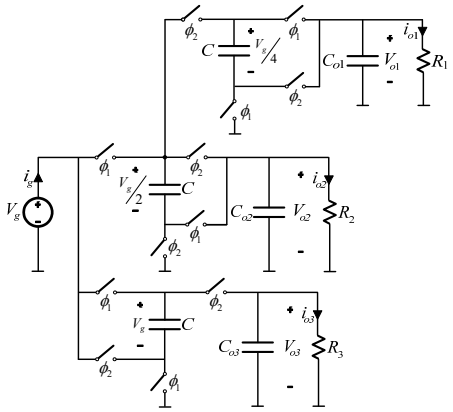


a) SC combination converter for M=2 and M=1/2 configuration.

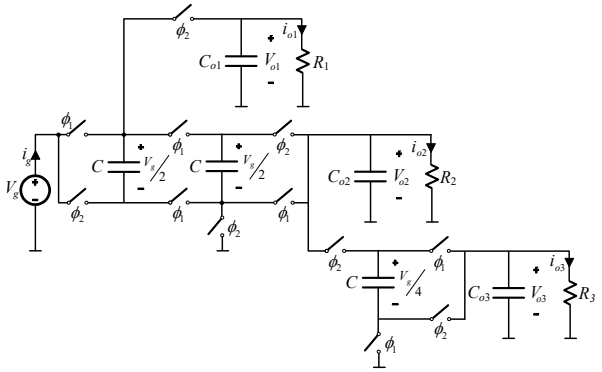


b) SC combination converter for M=3/2 and M=1/2 configuration.

Fig. 3. Two-output-type SC converters combination topologies.



a) SC combination converter for M=1/4, M=1/2 and M=2 configuration.



b) SC combination converter for M=3/2, M=1/2 and M=1/4 configuration.

Fig. 4. Three-output-type SC converters combination topologies.

Moreover, other combinations are also possible. If SC converters from Fig. 2 are combined, we can obtain single-input three-output converters, with step-down and step-up voltage ratios, as shown in Fig. 4. Both configurations are similar and implemented with twelve switches, and three link capacitors (controlled by two phase clocks ϕ_1 and ϕ_2), but provide different conversion ratios, step-up and step down (see Eqs. (4) and (5)).

$$\text{For Fig. 4(a):}\quad V_{o_1}=\frac{V_g}{4},\ V_{o_2}=\frac{V_g}{2}\ \text{and}\ V_{o_3}=2V_g \tag{4}$$

$$\text{For Fig. 4(b):}\quad V_{o_1}=\frac{3V_g}{2},\ V_{o_2}=\frac{V_g}{2}\ \text{and}\ V_{o_3}=\frac{V_g}{4} \tag{5}$$

The three-output type SC converters operate as follows: during the first half-period ϕ_1, the power supplied by the generator charges the link capacitors (C) through the switches connected to phase ϕ_1. Similarly, during the next half-period ϕ_2, the link capacitors (C) discharges into the load capacitors (C_{o1}, C_{o2} and C_{o3}) through the switches connected to phase ϕ_2. The on-resistance of the switches (R_{on}) influences the time constant for charging and discharging, and also a small amount of voltage is dropped across R_{on}. If it is assumed that R_{on} is negligible, then the voltages established in the link capacitors are those indicated in Fig. 4. For practical implementation, the three-output type combination topologies have some current load and the switches have a not negligible on-resistance, which results in small differences at the output voltages (V_{o1}, V_{o2} and V_{o3}) when compared to the ideal SC converter versions.

The last SC converter combination example intends to use more switches and link capacitors to obtain different output conversion ratios, in this case M=4/3 and M=1/3. Analyzing Fig. 5, five capacitors and eleven switches are required to realize the two outputs defined in equation (6).

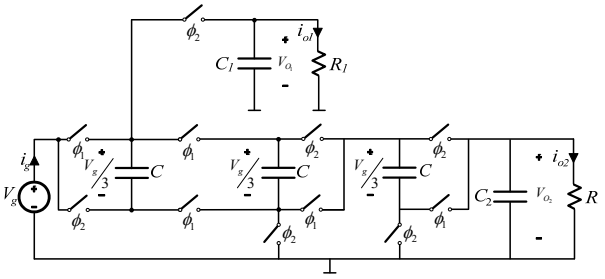


Fig. 5. Two-output-type SC converters combination topologies for M=4/3 and M=1/3.

$$\text{For Fig. 5:}\quad V_{o_1}=\frac{4V_g}{3}\ \text{and}\ V_{o_2}=\frac{V_g}{3} \tag{6}$$

It is important to note that this multiple-output versions are especially suited applications where a fully integration is required on the DC-DC converters and area is critical.

III. Simulation Results

In order to verify the behavior of the SC combination converters, simulations were carried out using Synopsys® HSPICE simulator tool. The test circuits were all implemented using a proprietary 65nm CMOS technology library, using PTM

(Predictive Technology Model) transistors obtained from Arizona State University [19]. Typical nominal conditions for this technology include V_{DD}=1.1V, with T=27ºC. Considering that one of the purposes of this paper is to define new DC-DC converter schemes for IoT applications, and that IoT requires ultra-low-power circuits that work with scalable power-supply voltages (that may include subthreshold voltages), it is important to state that, for the target technology used, the minimum working power-supply voltage is 0.16V (approximately V_{DD}/7).

The circuit used to generate the two-phase non-overlapping clock signals ϕ_1 and ϕ_2 is shown in Fig. 6. Considering the switches, both ideal and not ideal switches were used in the simulations, as will be explained. The transistor switches were implemented using a transmission gate (Fig. 7) (the transistors' size details will be described later on).

The first simulation results intend to make the proof-of-concept for the use of SC converters combined to implement single-input multiple-output, SC DC-DC converters. Therefore, in these first simulations, only ideal switches were used (switches with low R_{on}), as well as high load resistances (R_{Load} = 1 MΩ). In these conditions, capacitor values influence mostly the time to achieve the steady-state response and the output ripple. Therefore, 100 *f*F values were used on the link capacitors, and 2 *p*F values were used in the output capacitors. This assures that a low ripple is obtained with the high load resistances used. Note that, for all the converters simulated, the input voltage V_g is obtained from the available power-supply voltage, i.e., V_{DD} = 1.1 V.

Figs. 8, 9 and 10, present simulations for the proof-of-concept with the SC DC-DC converter circuits from, respectively, Figs. 2, 3 and 4. As it can be seen, despite the small V_{DD} voltage values used in the 65 nm target library, all the steady-state results obtained are very close to the ideal values described respectively in equations (1), (2), (3), (4) and (5). Moreover, and especially in the thee-output converters, the DC-DC converters obtained use less components, when compared to the corresponding single-output converters.

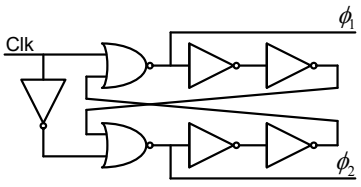


Fig. 6. Circuit to generate clock phases ϕ_1 and ϕ_2.

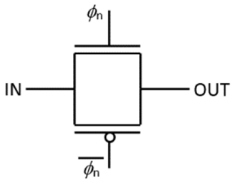
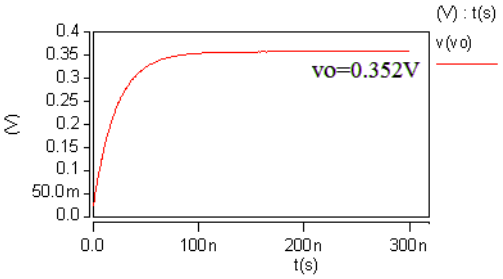
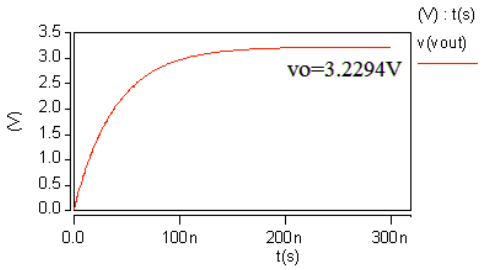


Fig. 7. Transmission gate switch.

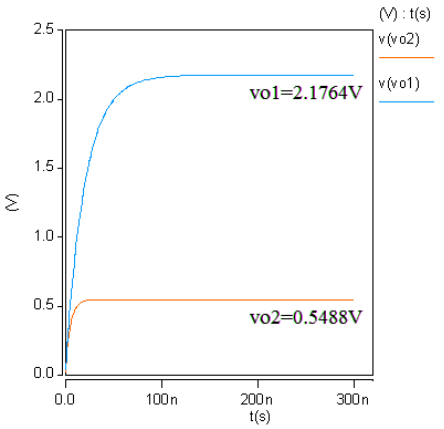


a) Simulation results for Fig. 2.a) configuration: $V_o = V_g/3$.

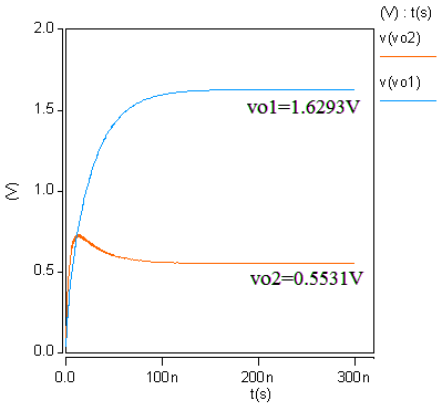


b) Simulation results for Fig. 2.b) configuration: $V_o = V_g/3$.

Fig. 8. Simulation results for Fig. 2 topologies.

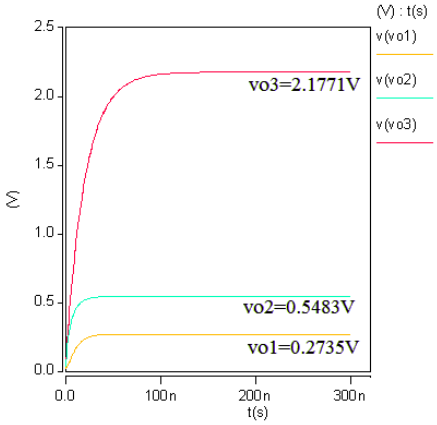


a) Simulation results for Fig. 3.a) configuration with M=2 and *M*=1/2.

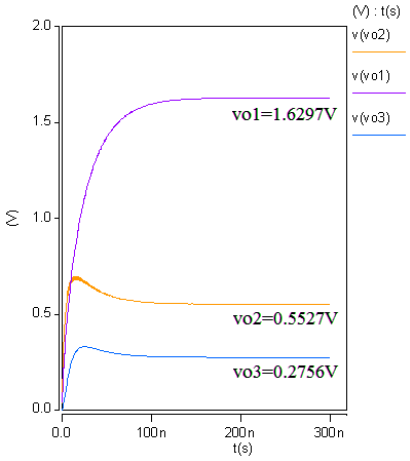


b) Simulation results for Fig. 3.b) configuration with *M*=3/2 and *M*=1/2.

Fig. 9. Simulation results for Fig. 3 three output topologies.



a) Simulation results for Fig. 4.a) configuration, with M=1/4, M=1/2 and M=2.



b) Simulation results for Fig. 4.b) configuration, with M=3/2, M=1/2 and M=1/4.

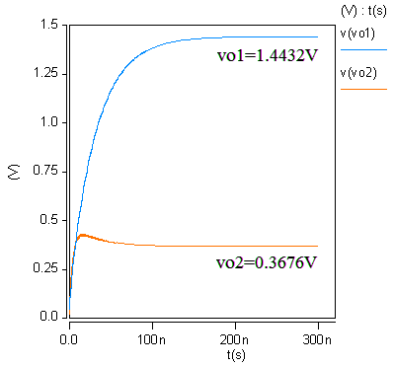
Fig. 10. Simulation results for Fig. 4 three output topologies.

The next simulation results intend to analyze, for the configuration in Fig. 5, a real on-chip situation and typical application for the converter. Therefore, instead of ideal switches and high resistance loads as in the previous simulations, transistor switches and load resistances with R_{Load} = 100 kΩ were used. The transistor-based switches were implemented with Fig. 7 transmission gates with transistors' sizes defined in (7), and with multiplicity of seven (i.e, seven identical transistors in parallel, to reduce the on-resistance of the switches).

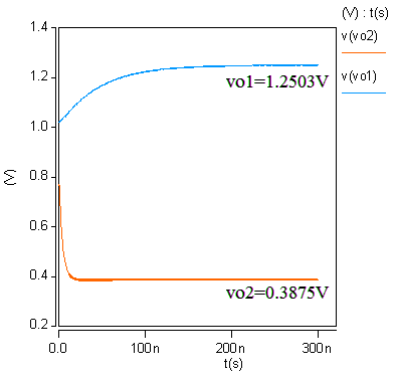
$$W_N = 5W_{Nmin};\ L_N=2L_{Nmin};\ W_P = 13W_{Pmin};\ L_P=2L_{Pmin} \quad (7)$$

Regarding the capacitors sizes, the values were chosen to minimize output voltage error (when compared with the ideal output voltage) and maintaining the output ripple low. The values used were: C =3 pF, C_1=20 pF, and C_2 = 5 pF.

Fig. 11 present the results for the ideal situation (Fig. 11.a)) and the real, on-chip, situation (Fig. 11.b)). These results show that it is possible to implement these combined SC DC-DC converters in nanometer technologies.



a) With ideal switches and R_{Load} = 1 MΩ.



b) With transistor switches and R_{Load} = 100 kΩ.

Fig. 11. Simulation for Fig. 7 SC converter circuit (M=4/3 and M=1/3).

Although the previous simulation use real transistor switches, it also uses high load resistances, which is still close to an ideal situation. In a multiple-output SC DC-DC circuit, one problem is to tune all the parameters to a good output result for all the outputs simultaneously, and the problem worsens when the output power is increased. So, let us consider the 2 output SC combination of Fig. 12. Here, by combining the two circuits to generate both outputs in the same circuit, 4 switches and 2 capacitors are avoided, when compared with two individual SC circuits that could generate the same two outputs. Here, the Vo1 output with Vg/4 is generated using a Vg/2 signal, obtained in Vo2 circuit. Moreover, let us consider 1kΩ load resistances in each output, to create a real load situation. Nevertheless, it is important to mention that these SoC low-voltage DC-DC circuits are for IoT ultra-low power applications.

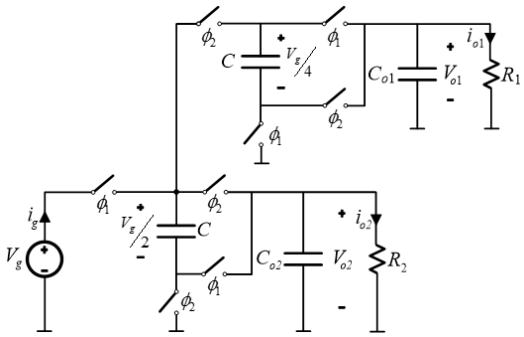


Fig. 12. SC combination converter for M=1/4 and M=1/2 configuration.

The results obtained are presented in Fig. 13, and the circuit obtained has 58,5% of efficiency, with 0.357mW of output power, with two simultaneous outputs for 0.505V and 0.32V, each one with a 1kΩ load. The switches used a 2GHz clock frequency, and as shown in Fig. 14, the switching current in the input voltage source (which is the same for the input switch) as a maximum current of 5mA. It is also important to mention that in these SC combinations, no inductors are used and all circuits can be fully integrated in a SoC.

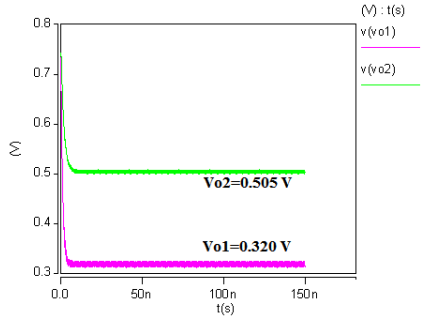


Fig. 13. Simulation for Fig. 12 SC converter circuit (M=1/4 and M=1/2).

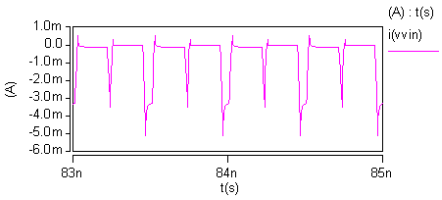


Fig. 14. Simulation for switching current in Vg (M=1/4 and M=1/2).

IV. Conclusions

This paper presents switched-capacitor DC-DC combination converters with single-input, two and three-outputs, with step-down and step-up voltage ratios. The combination converters provide different DC outputs, with different conversion ratios. The main advantage of the proposed converters is the low number of components used in the combination, two-outputs combination configurations require two link capacitors, and three-outputs combination configurations require three link capacitors, and only two complemented square signals are necessary, which reduces their sizes and manufacturing costs. Many applications require step-down, step-up and/or multiple/different outputs from the same power supply. An analysis of the proposed configurations for different conditions has been carried out. Simulation results show that these combination converter topologies are suitable for multiple output-type switched-capacitor DC-DC converters with different conversion ratio.

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